DS26502DK
T1/E1/J1/64KCC Bits Element Design Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS26502DK is an easy-to-use evaluation board for the DS26502 T1/E1/J1/64KCC BITS element. The DS26502DK is intended to be used as a stand-alone design kit. The board is complete with a DS26502 BITS element, transformers, termination resistors, FPGA-based configuration switches, and network connectors. Dallas' ChipView software gives point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status as well as multiple clock and signal routing configurations.

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DESIGN KIT CONTENTS

DS26502DK Design Kit
CD_ROM Including:

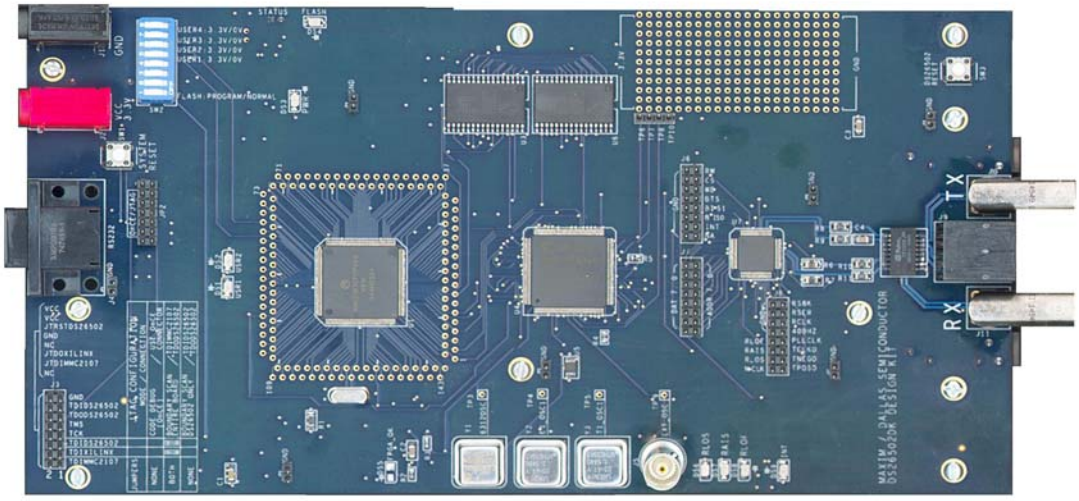
- ChipView Software
- DS26502DK Data Sheet
- DS26502 Data Sheet
- DS26502 Errata Sheet (if applicable)

ORDERING INFORMATION

PART	DESCRIPTION
DS26502DK	Stand-Alone Design Kit for DS26502

FEATURES

- **Expedites New Designs by Eliminating First-Pass Prototyping**
- **Demonstrates Key Functions of DS26502 BITS Element**
- **Includes DS26502 BITS Element, Transformers, BNC, and RJ48 Network Connectors and Termination Passives**
- **BNC Connections for 75Ω E1**
- **Bantam and RJ48 Connectors for 120Ω E1 and 100Ω T1**
- **Interface Directly to Windows-Based Computers**
- **ChipView Software Provides Point-and-Click Access to the DS26502 Register Set**
- **Software Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing**
- **All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink**
- **LEDs for Loss-of-Signal and Interrupt Status as well as Indications for Multiple Clock and Signal Routing Configurations**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

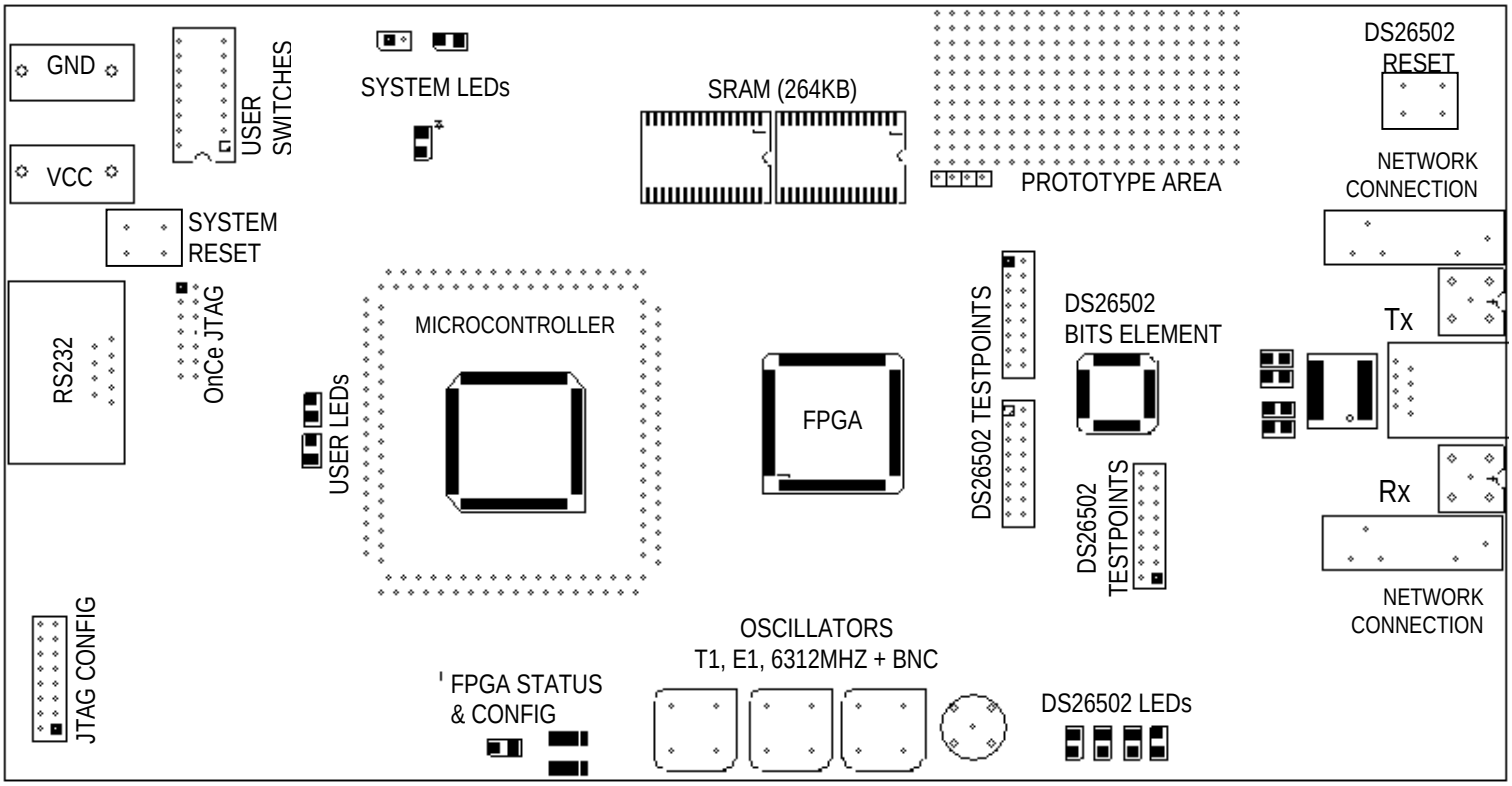


COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1, C4, C23, C51, C53	5	10µF 20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
C2–C3, C6–C9, C11, C12, C14, C15, C17, C18, C20, C21, C25–C30, C32, C33, C35, C36, C38, C45–C50, C52, C54, C55, C57–C60, C62, C63, C68	41	1µF 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
C5, C10, C22, C24, C31, C34, C37, C39–C41, C43, C65–C67, C69, C70	16	0.1µF 20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
C13, C19, C42, C44, C64	5	10µF 20%, 16V tantalum capacitors (B case)	Panasonic	ECS-T1CX106R
C16, C56, C61	3	68µF 20%, 16V tantalum capacitors (D case)	Panasonic	ECS-T1CD686R
D1	1	1A 50V general-purpose silicon diode	General Semiconductor	1N4001
DS1, DS2, DS6–DS9	6	LED, RED, SMD	Panasonic	LN1251C
DS3	1	LED, GREEN, SMD	Panasonic	LN1351C
DS4	1	LED, AMBER, SMD	Panasonic	LN1451C
DS5	1	LED, GREEN, SMD (Not populated)	Panasonic	LN1351C
DS10	1	LED red/green, 5mm red/green right-angle PCMT	Digi-Key	350-1055-ND
J1	1	Socket, banana plug, horizontal, black	Mouser Electronics	164-6218
J2	1	Socket, banana plug, horizontal, red	Mouser Electronics	164-6219
J3, J6–J8	4	Terminal strip, 16-pin, dual row, vertical	Samtec	TSW-108-07-T-D
J4	1	DB9 right-angle, long case connector	AMP	747459-1
J5	1	L_CONNECTOR BNC 75Ω vertical 5-pin	Cambridge	CP-BNCPC-004
J9	1	L_RJ48 8-pin, single-port connector	MOLEX	15-43-8588
J10, J11	2	BNC connectors, 75Ω right-angle 5-pin	Kruvand	UCBJR220
J12, J13	2	L_CONN, Bantam jack, right-angle	Switchcraft	RTT34B02
JP1, JP3–JP8	7	100-mil, 2 position jumper	labstock	
JP2	1	14-pin header, remove 'missing pin'	labstock	
L1	1	Inductor, 22.0µH 2-pin SMT 20%	Coiltronics	UP1B-220
NP1, NP2	2	10pF 5%, 50V tall case ceramic capacitors (1206) Do not populate	Phycomp	1206CG100J9B200
R1, R8–R11	5	0Ω 5%, 1/8W resistors (1206)	Panasonic	ERJ-8GEYJ0R00V
R2, R13, R23, R27, R43, R47, R67–R70	10	330Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R3, R18–R20, R22, R25, R26, R28–R31, R33–R42, R44–R46, R49, R50, R53, R56, R59, R61, R62, R65, R72	33	10kΩ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
R4, R5, R48, R51, R54, R55, R57, R58	8	30Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ300V
R6, R7	2	61.9Ω 1%, 1/8W resistors (1206)	Panasonic	ERJ-8ENF61R9V
R12	1	51Ω 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ510V
R14–R17, R21, R24, R63, R64, R66, R71	10	1.0kΩ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ102V
R32	1	1.0kΩ 5%, 1/10W resistor (0805)	Panasonic	ERJ-6GEYJ102V
R52	1	51.1Ω 1%, 1/10W resistor (0805)	Panasonic	ERJ-6ENF51R1V
R60	1	1.0MΩ 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ105V
SW1, SW3	2	Switch MOM 4-pin single pole	Panasonic	EVQPAE04M
SW2	1	Switch 8-position, 16-pin DIP, low profile	AMP	435668-7
T1	1	XFMR 16P SMT	Pulse	TX1099
TP1, TP2	2	Testpoint, 1 plate thru-hole	NA	NA
TP3–TP10	8	Testpoint, 1 plated hole DO NOT STUFF	NA	NA
U1	1	32-bit microcontroller (lab stock)	Avnet	MMC2107CFCV33
U3, U6	2	SRAM 5V, 1Mb SO (in lab stock)	Cypress	CY62128V
U4	1	Xilinx Spartan 2.5V FPGA, 20mm x 20mm 144-pin TQFP	Xilinx	XC2S50-5TQ144C
U5	1	8-Pin μMAX/SO 2.5V or Adj	Maxim	MAX1792EUA25
U7	1	64-pin LQFP T1/E1/J1 BITS element (0°C to +70°C)	Dallas Semiconductor	DS26502L
U8, U9, U13	3	High-speed inverter	Fairchild	NC7SZ86
U10	1	High-speed buffer	Fairchild	NC7SZ86
U11	1	Dual RS-232 transceivers with 3.3V/5V internal capacitors	Maxim	MAX3233E
U12	1	1Mb flash-based config mem	Xilinx	XCF01SV020C
U14	1	8-pin SO step-up DC-DC converter 0.5A limit	Maxim	MAX1675EUA
X1	1	Low-profile 8.0MHz crystal	PEI	EC1-8.000M
Y1	1	Oscillator, crystal clock, 3.3V, 6.312MHz	SaRonix	NTH069A3-6.312
Y2	1	Oscillator, crystal clock, 3.3V, 2.048MHz	SaRonix	NTH039A3-2.0480
Y3	1	Oscillator, crystal clock, 3.3V, 1.544MHz	SaRonix	NTH039A3-1.5440

BOARD FLOORPLAN



ERRATA

The design kit errata refer to two difference PC board revisions: the DS26502DK01A0 and DS26502DK01B0. The PC board revision code is found on the bottom of the board in the lower right corner.

DS26502DK01A0 Circuit Boards

- RCLK did not get connected to FPGA. A jumper wire was run from RCLK to TP10 to provide the connection.
- Silkscreen for J3.4 is incorrect. Silkscreen reads “JTD**I**MMC2107” and should read “JTD**O**MMC2107.”
- RJ45 connector J4 does not use the standard pin numbers for connection to the transformer (and subsequently to TTIP/TRING and RTIP/RRING). This connector has been left unpopulated to avoid confusion. The schematic has been updated and is correct.
- DC blocking capacitor C4 on TTIP too small. A 10μF capacitor is recommended; a 1μF capacitor was populated.

DS26502DK01B0 Circuit Boards

- RJ45 connector J4 does not use the standard pin numbers for connection to the transformer (and subsequently to TTIP/TRING and RTIP/RRING). This connector has been left unpopulated to avoid confusion. The schematic has been updated and is correct.

ADDITIONS

The following signals have been connected to Testpoints via the FPGA:

- TP6 is driven with data present at the TS_8K_4 pin of the DS26502.
- TP7 is driven with the 400Hz signal mentioned in the TS_8Ksrc register (page 15).
- TP8 is driven with the 8KHz signal mentioned in the TS_8Ksrc register (page 15).

BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/telecom. See the DS26502DK QuickView data sheet for these files.

Hardware Configuration

- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V.
- DIP switches are unused and can be in either the ON or OFF position with exception for the Flash programming switch, which should be OFF.
- From the Programs menu, launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.

General

- Upon power-up the RLOS and RLOF LEDs (red) will be lit, the INT LED (red) will not be lit, and Status LED (DS10 red/green bicolor) will be green.

Quick Setup (Register View)

- The PC will load ChipView offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select Register View.
- The program will then request a definition file. Select DS26502DC_FPGA.def. Through the 'links' section, this will also load DS26502.def.
- The Register View Screen will appear, showing the register names, acronyms, and values for the DS26502.
- Predefined Register settings for several functions are available as initialization files.
  - ini files are loaded by selecting the menu File→Reg ini File→Load ini File.
  - Load the ini file "CompositeClock.ini."
  - Load the ini file "DS26502FPGA_2048Clks.ini," which sets the DS26502 in Intel nonmultiplexed mode with MCLK driven at 2.048MHz.
  - After loading the ini files the following may be observed:
    - The RLOS and RLOF LEDs extinguishes upon external loopback.
    - The part begins operating in composite clock mode.

Miscellaneous

- Clock frequencies and certain pin bias levels are provided by a register-mapped FPGA.
- The definition file for this FPGA is named DS26502DC_FPGA.def. The FPGA register definitions are located on page 6. A drop-down menu on the top of the screen allows for switching between definition files.
- All files referenced above are available for download as described in the section marked "BASIC OPERATION."

ADDRESS MAP

Device address space (DS26502 and FPGA) begins at 0x81000000.

All offsets given below are relative to the beginning of the device address space (shown above).

Table 1. Device Address Map

OFFSET	DEVICE	DESCRIPTION
0x0000 to 0x0030	FPGA	Board identification and clock/signal routing
0x8000 to 0x80ff	DS26502 T1/E1/J1 BITS element	DS26502 T1/E1/J1 BITS element

Registers in the FPGA can be easily modified using the ChipView host-based user interface software along with the definition file named “DS26502DC_FPGA.def”.

FPGA Register Map

Table 2. FPGA Register Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0x0000	BID	Read only	BOARD ID
0x0001	Unused	—	—
0x0002	XBIDH	Read only	HIGH NIBBLE EXTENDED BOARD ID
0x0003	XBIDM	Read only	MIDDLE NIBBLE EXTENDED BOARD ID
0x0004	XBIDL	Read only	LOW NIBBLE EXTENDED BOARD ID
0x0005	BREV	Read only	BOARD FAB REVISION
0x0006	AREV	Read only	BOARD ASSEMBLY REVISION
0x0007	PREV	Read only	PLD REVISION
0x0007	BUSMO	Read only	BUS MODE INFORMATION
0x09-0x10	Unused	—	—
0x0011	LEVEL1	Control	DS26502 pin settings (THZE, BTS–HBE, BIS1, BIS0)
0x0012	LEVEL2	Control	DS26502 pin settings (RMODE3, RMODE2, RMODE1, RMODE0)
0x0013	LEVEL3	Control	DS26502 pin settings (RSM, RITD)
0x0014	LEVEL4	Control	DS26502 pin settings (TSM, TITD)
0x0015	LEVEL5	Control	DS26502 pin settings (TCSS1, TCSS0)
0x0016	LEVEL6	Control	DS26502 pin settings (TMODE3, TMODE2, TMODE1, TMODE0)
0x0017	LEVEL7	Control	DS26502 pin settings (L2, L1, L0)
0x0018	LEVEL8	Control	DS26502 pin settings (TAIS, RLB)
0x0019	LEVEL9	Control	DS26502 pin settings (MPS1, MPSO)
0x001A	LEVEL10	Control	DS26502 pin settings (JAMUX, E1TS)
0x001B	Unused	—	—
0x001C	TSERsrc	Control	DS26502 TSER source selection
0x001D	MCLKsrc	Control	DS26502 MCLK source selection
0x001E	TCLK	Control	DS26502 TCLK source selection
0x001F	TS_8K	Control	DS26502 TS_8K source selection
0x0020	Unused	—	—
0x0021	Unused	—	—

FPGA ID Registers

BID: BOARD ID (Offset = 0x0000)

BID is read only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0x0002)

XBIDH is read only with a value of 0x0.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0x0003)

XBIDM is read only with a value of 0x1.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0x0004)

XBIDL is read only with a value of 0x6.

BREV: BOARD FAB REVISION (Offset = 0x0005).

BREV is read only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset = 0x0006)

AREV is read only and displays the current assembly revision.

PREV: PLD REVISION (Offset = 0x0007)

PREV is read only and displays the current PLD firmware revision.

FPGA Status Registers

Register Name: **BUSMO**
Register Description: **DS26502 Bus Mode**
Register Offset: **0x0011**

Bit #	7	6	5	4	3	2	1	0
Name	LevCPOL	LevCPHA	HW	SPI	INMUX	IMUX	MNMUX	MMUX
Default	—	—	—	—	—	—	—	—

The FPGA derives values in the BUSMO register from the levels present at the DS26502 pins.

Bit 7: LevCPOL. When set the DS26502 CPOL pin is high. Note: This pin is called A3/CPOL/L1 in parallel/serial/hardware modes.

Bit 6: LevCPHA. When set the DS26502 CPHA pin is high. Note: This pin is called A2/CPHA/L0 in parallel/serial/hardware modes.

Bit 5: HW. When set the DS26502 is in hardware mode.

Bit 4: SPI. When set the DS26502 is in SPI (3-wire) mode.

Bit 3: INMUX. When set the DS26502 is in Intel nonmultiplexed mode.

Bit 2: IMUX. When set the DS26502 is in Intel multiplexed mode.

Bit 1: MNMUX. When set the DS26502 is in Motorola nonmultiplexed mode.

Bit 0: MMUX. When set the DS26502 is in Motorola multiplexed mode.

FPGA Control Registers

The FPGA register set consists of two types of registers: level setting and clock multiplexing. There are 10 registers for tri-state and level-control setting when in hardware mode. The level-setting registers are only valid when the DS26502 is in hardware mode (BIS1:0 = 11). When in nonhardware mode, the FPGA pins affected by the level registers are automatically either tri-stated, or assume an alternate function (e.g., they function as address databus pins or SPI pins). Exceptions are given with the register descriptions.

Register Name: **LEVEL1**
Register Description: **DS26502 Pin Settings (THZE, BTS, BIS1, BIS0)**
Register Offset: **0x0011**

Bit #	7	6	5	4	3	2	1	0
Name	THZEtri	THZE_Lev	BTStri	BTS_Lev	BIS1tri	BIS1_Lev	BIS0tri	BIS0_Lev
Default	0	0	0	0	0	0	0	1

Note: *This register is only valid in ALL modes (many of the level registers are only valid in hardware mode).*

Bits 7 and 6: DS26502 THZE Tri-State and Level (THZEtri and THZE_Lev)
00 = FPGA drives THZE with 0V
01 = FPGA drives THZE with 3.3V
1x = FPGA tri-states THZE pin

Bit 5 and 4: DS26502 BTS Tri-State and Level (BTStri and BTS_Lev)
00 = FPGA drives BTS with 0V
01 = FPGA drives BTS with 3.3V
1x = FPGA tri-states BTS pin

Bits 3 and 2: DS26502 BIS1 Tri-State and Level (BIS1tri and BIS1_Lev)
00 = FPGA drives BIS1 with 0V
01 = FPGA drives BIS1 with 3.3V
1x = FPGA tri-states BIS1 pin

Bits 1 and 0: DS26502 BIS0 Tri-State and Level (BIS0tri and BIS0_Lev)
00 = FPGA drives BIS0 with 0V
01 = FPGA drives BIS0 with 3.3V
1x = FPGA tri-states BIS0 pin

Register Name: **LEVEL2**
Register Description: **DS26502 Pin Settings (RMODE3, RMODE2, RMODE1, RMODE0)**
Register Offset: **0x0012**

Bit #	7	6	5	4	3	2	1	0
Name	RMODE3 tri	RMODE3 _Lev	RMODE2 tri	RMODE2 _Lev	RMODE1 tri	RMODE1 _Lev	RMODE0 tri	RMODE0 _Lev
Default	0	0	0	0	0	0	0	0

Note: *This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.*

Bits 7 and 6: DS26502 RMODE3 Tri-State and Level (RMODE3tri and RMODE3_Lev)
00 = FPGA drives RMODE3 with 0V
01 = FPGA drives RMODE3 with 3.3V
1x = FPGA tri-states RMODE3 pin

Bits 5 and 4: DS26502 RMODE2 Tri-State and Level (RMODE2tri and RMODE2_Lev)
00 = FPGA drives RMODE2 with 0V
01 = FPGA drives RMODE2 with 3.3V
1x = FPGA tri-states RMODE2 pin

Bits 3 and 2: DS26502 RMODE1 Tri-State and Level (RMODE1tri and RMODE1_Lev)
00 = FPGA drives RMODE1 with 0V
01 = FPGA drives RMODE1 with 3.3V
1x = FPGA tri-states RMODE1 pin

Bits 1 and 0: DS26502 RMODE0 Tri-State and Level (RMODE0tri and RMODE0_Lev)
00 = FPGA drives RMODE0 with 0V
01 = FPGA drives RMODE0 with 3.3V
1x = FPGA tri-states RMODE0 pin

Register Name: **LEVEL3**
Register Description: **DS26502 Pin Settings (RSM, RITD)**
Register Offset: **0x0013**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RSMtri	RSM _Lev	—	—	RITDtri	RITD_Lev
Default	0	0	0	0	0	0	0	0

Note: *This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.*

Bits 5 and 4: DS26502 RSM Tri-State and Level (RSMtri and RSM _Lev)
00 = FPGA drives RSM with 0V
01 = FPGA drives RSM with 3.3V
1x = FPGA tri-states RSM pin

Bits 1 and 0: DS26502 RITD Tri-State and Level (RITDtri and RITD_Lev)
00 = FPGA drives RITD with 0V
01 = FPGA drives RITD with 3.3V
1x = FPGA Tristates RITD pin

Register Name: **LEVEL4**
Register Description: **DS26502 Pin Settings (TSM, TITD)**
Register Offset: **0x0014**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TSMtri	TSM_Lev	—	—	TITDtri	TITD_Lev
Default	0	0	0	0	0	0	0	0

Note: *This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.*

Bits 5 and 4: DS26502 TSM Tri-State and Level (TSMtri and TSM_Lev)
00 = FPGA drives TSM with 0V
01 = FPGA drives TSM with 3.3V
1x = FPGA tri-states TSM pin

Bits 1 and 0: DS26502 TITD Tri-State and Level (TITDtri and TITD_Lev)
00 = FPGA drives TITD with 0V
01 = FPGA drives TITD with 3.3V
1x = FPGA tri-states TITD pin

Register Name: **LEVEL5**
Register Description: **DS26502 Pin Settings (TCSS1, TCSS0)**
Register Offset: **0x0015**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TCSS1tri	TCSS1_Lev	—	—	TCSS0tri	TCSS0_Lev
Default	0	0	0	0	0	0	0	0

Note: *This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.*

Bits 5 and 4: DS26502 TCSS1 Tri-State and Level (TCSS1tri and TCSS1_Lev)
00 = FPGA drives TCSS1 with 0V
01 = FPGA drives TCSS1 with 3.3V
1x = FPGA tri-states TCSS1 pin

Bits 1 and 0: DS26502 TCSS0 Tri-State and Level (TCSS0tri and TCSS0_Lev)
00 = FPGA drives TCSS0 with 0V
01 = FPGA drives TCSS0 with 3.3V
1x = FPGA tri-states TCSS0 pin

Register Name: **LEVEL6**
Register Description: **DS26502 Pin Settings (TMODE3, TMODE2, TMODE1, TMODE0)**
Register Offset: **0x0016**

Bit #	7	6	5	4	3	2	1	0
Name	TMODE3 tri	TMODE3 _Lev	TMODE2 tri	TMODE2 _Lev	TMODE1 tri	TMODE1 _Lev	TMODE0 tri	TMODE0 _Lev
Default	0	0	0	0	0	0	0	0

Note: *This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.*

Bits 7 and 6: DS26502 TMODE3 Tri-State and Level (TMODE3tri and TMODE3_Lev)
00 = FPGA drives TMODE3 with 0V
01 = FPGA drives TMODE3 with 3.3V
1x = FPGA tri-states TMODE3 pin

Bits 5 and 4: DS26502 TMODE2 Tri-State and Level (TMODE2tri and TMODE2_Lev)
00 = FPGA drives TMODE2 with 0V
01 = FPGA drives TMODE2 with 3.3V
1x = FPGA tri-states TMODE2 pin

Bits 3 and 2: DS26502 TMODE1 Tri-State and Level (TMODE1tri and TMODE1_Lev)
00 = FPGA drives TMODE1 with 0V
01 = FPGA drives TMODE1 with 3.3V
1x = FPGA tri-states TMODE1 pin

Bits 1 and 0: DS26502 TMODE0 Tri-State and Level (TMODE0tri and TMODE0_Lev)
00 = FPGA drives TMODE0 with 0V
01 = FPGA drives TMODE0 with 3.3V
1x = FPGA tri-states TMODE0 pin

Register Name: **LEVEL7**
Register Description: **DS26502 Pin Settings (L2, L1, L0)**
Register Offset: **0x0017**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	L2tri	L2_Lev	L1tri	L1_Lev	L0tri	L0_Lev
Default	0	0	0	0	0	0	0	0

Note: *Settings for L2 are only valid in hardware mode (BIS[1:0] = 11), and ignored for other modes. In serial mode (BIS[1:0] = 10), L0 and L1 are used to set levels for CPHA and CPOL, respectively.*

Bits 5 and 4: DS26502 L2 Tri-State and Level (L2tri and L2_Lev)
00 = FPGA drives L2 with 0V
01 = FPGA drives L2 with 3.3V
1x = FPGA tri-states L2 pin

Bits 3 and 2: DS26502 L1 Tri-State and Level (L1tri and L1_Lev)
00 = FPGA drives L1 with 0V
01 = FPGA drives L1 with 3.3V
1x = FPGA tri-states L1 pin

Bits 1 and 0: DS26502 L0 Tri-State and Level (L0tri and L0_Lev)
00 = FPGA drives L0 with 0V
01 = FPGA drives L0 with 3.3V
1x = FPGA tri-states L0 pin

Register Name: **LEVEL8**
Register Description: **DS26502 Pin Settings (TAIS, RLB)**
Register Offset: **0x0018**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TAIS tri	TAIS_Lev	—	—	RLBtri	RLB_Lev
Default	0	0	0	0	0	0	0	0

Note: *This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.*

Bits 5 and 4: DS26502 TAIS Tri-State and Level (TAIS tri and TAIS_Lev)
00 = FPGA drives TAIS with 0V
01 = FPGA drives TAIS with 3.3V
1x = FPGA tri-states TAIS pin

Bits 1 and 0: DS26502 RLB Tri-State and Level (RLBtri and RLB_Lev)
00 = FPGA drives RLB with 0V
01 = FPGA drives RLB with 3.3V
1x = FPGA tri-states RLB pin

Register Name: **LEVEL9**
Register Description: **DS26502 Pin Settings (MPS1, MPSO)**
Register Offset: **0x0019**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	MPS1tri	MPS1_Lev	—	—	MPSOtri	MPSO_Lev
Default	0	0	0	0	0	0	0	0

Bits 5 and 4: DS26502 MPS1 Tri-State and Level (MPS1tri and MPS1_Lev)
00 = FPGA drives MPS1 with 0V
01 = FPGA drives MPS1 with 3.3V
1x = FPGA tri-states MPS1 pin

Bits 1 and 0: DS26502 MPS0 Tri-State and Level (MPSOtri and MPSO_Lev)
00 = FPGA drives MPS0 with 0V
01 = FPGA drives MPS0 with 3.3V
1x = FPGA tri-states MPS0 pin

Register Name: **LEVEL10**
Register Description: **DS26502 Pin Settings (JAMUX, E1TS)**
Register Offset: **0x000A**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	JAMUXtri	JAMUX_Lev	—	—	E1TStri	E1TS_Lev
Default	0	0	0	0	0	0	0	0

Note: *This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.*

Bits 5 and 4: DS26502 JAMUX Tri-State and Level (JAMUXtri and JAMUX_Lev)
00 = FPGA drives JAMUX with 0V
01 = FPGA drives JAMUX with 3.3V
1x = FPGA tri-states JAMUX pin

Bits 1 and 0: DS26502 E1TS Tri-State and Level (E1Tstri and E1TS_Lev)
00 = FPGA drives E1TS with 0V
01 = FPGA drives E1TS with 3.3V
1x = FPGA tri-states E1TS pin

Register Name: **TSERsrc**
Register Description: **DS26502 TSER Pin Source**
Register Offset: **0x001C**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	ZEROS	ONES	RSER
Default	0	0	0	0	0	0	1	0

Note: *Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to TSER. Setting to 0 also tri-states this pin.*

Bit 2: ZEROS. When set DS26502_TSER ← 0.0V.

Bit 1: ONES. When set DS26502_TSER ← 3.3V.

Bit 0: RSER. When set DS26502_TSER ← DS26502_RSER.

Register Name: **MCLKsrc**
Register Description: **DS26502 MCLK Pin Source**
Register Offset: **0x001D**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	ZERO	EXT	T1	E1
Default	0	0	0	0	0	0	1	0

Note: *Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to MCLK. Setting to 0 also tri-states this pin.*

Bit 3: ZERO. When set DS26502_ MCLK ← 0.0V.

Bit 2: EXT. When set DS26502_ MCLK ← External_Osc (BNC connector).

Bit 1: T1. When set DS26502_ MCLK ← T1_OSC (1.544MHz).

Bit 0: E1. When set DS26502_ MCLK ← E1_OSC (2.048MHz).

Register Name: **TCLKsrc**
Register Description: **DS26502 TCLK Pin Source**
Register Offset: **0x001E**

Bit #	7	6	5	4	3	2	1	0
Name	—	EXT	T1	E1	64KHZ	6312	PLL	RCLK
Default	0	0	1	0	0	0	0	0

Note: *Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to TCLK. Setting to 0 also tri-states this pin.*

Bit 6: EXT. When set DS26502_ TCLK ← External_Osc (BNC connector).

Bit 5: T1. When set DS26502_ TCLK ← T1_OSC (1.544MHz).

Bit 4: E1. When set DS26502_ TCLK ← E1_OSC (2.048MHz).

Bit 3: 64KHZ. When set DS26502_ TCLK ← 64kHz clock.

Bit 2: 6312. When set DS26502_ TCLK ← 6312kHz clock.

Bit 1: PLL. When set DS26502_ TCLK ← DS26502_PLL.

Bit 0: RCLK. When set DS26502_ TCLK ← DS26502_RCLK.

Register Name: **TS_8Ksrc**
Register Description: **DS26502 TS_8K Pin Source**
Register Offset: **0x001F**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	EXT	_8KHz	400HZ	400HZ_502	RS_8K
Default	0	0	0	0	0	0	1	0

Note: *Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to TS_8K. Setting to 0 also tri-states this pin.*

Bit 4: EXT. When set DS26502_TS_8K ← External_Osc (BNC connector).

Bit 3: _8KHz. When set DS26502_TS_8K ← 8kHz (derived by FPGA).

Bit 2: 400HZ. When set DS26502_TS_8K ← 400Hz clock (derived by FPGA).

Bit 1: 4KHZ_502. When set DS26502_TS_8K ← DS26502_400hz.

Bit 0: RS_8K. When set DS26502_TS_8K ← DS26502_RS_8K.

DS26502 INFORMATION

For more information about the DS26502, consult the DS26502 data sheet available on our website at www.maxim-ic.com/DS26502. Software downloads are also available for this design kit.

DS26502DK INFORMATION

For more information about the DS26502DK, including software downloads, consult the DS26502DK data sheet available on our website at www.maxim-ic.com/DS26502DK.

TECHNICAL SUPPORT

For additional technical support, go to www.maxim-ic.com/support.

SCHEMATICS

The DS26502DK schematics are featured in the following pages.

DOCUMENT REVISION HISTORY

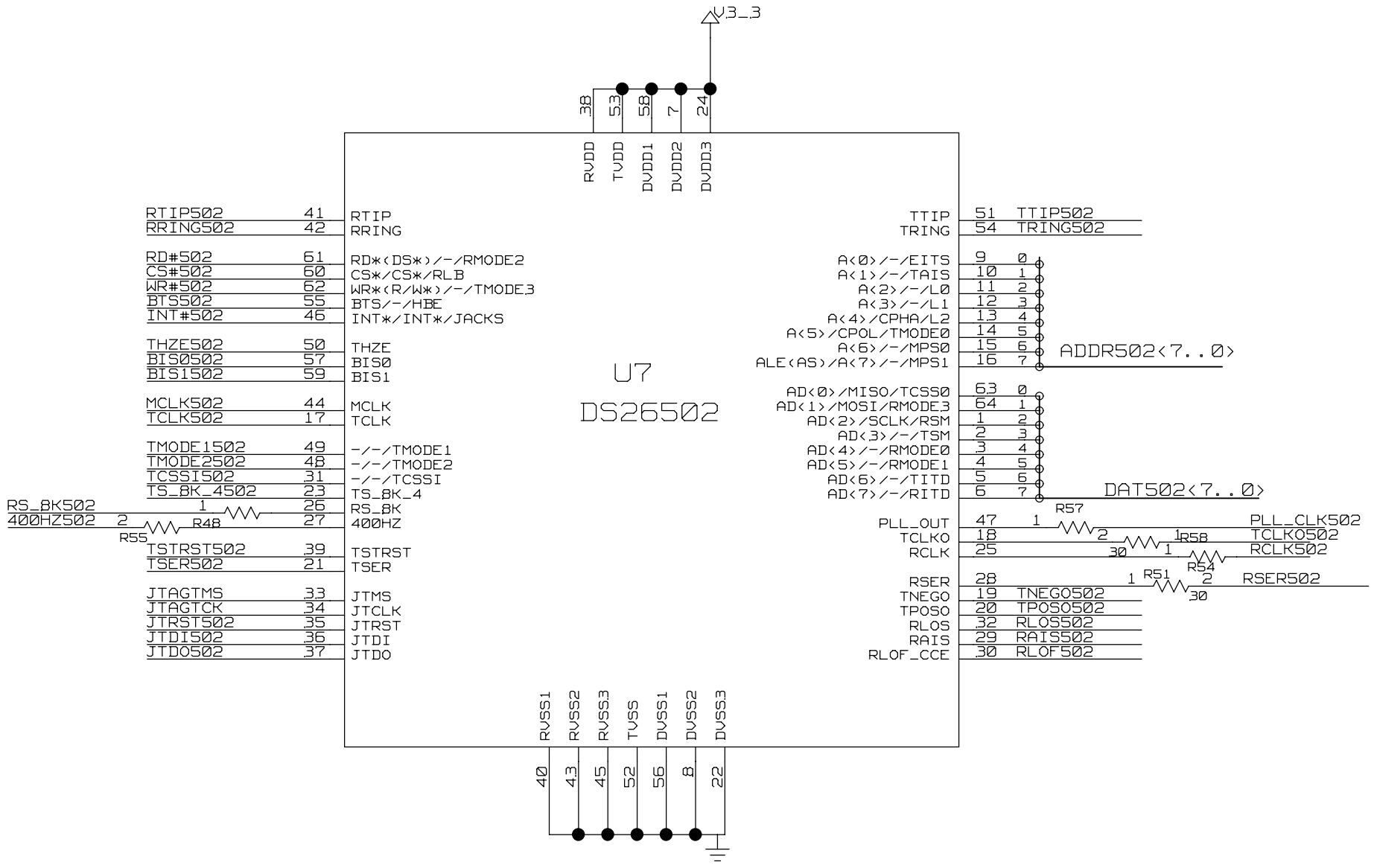
REVISION DATE	DESCRIPTION
030705	Initial DS26502DK data sheet release.
070505	Updated *Features*, *Component List* (lines 1 and 2), and *Errata* sections.
071006	Updated descriptions for FPGA Control Registers LEVEL1 to LEVEL10.
110106	Updated schematics.
031507	Corrected typo on Bit 0 of TSERsrc register Corrected typo on Bit 0 of TS_8Ksrc register

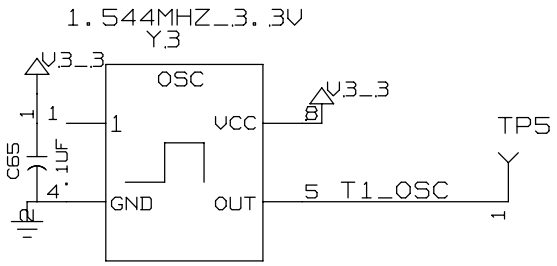
DS26502

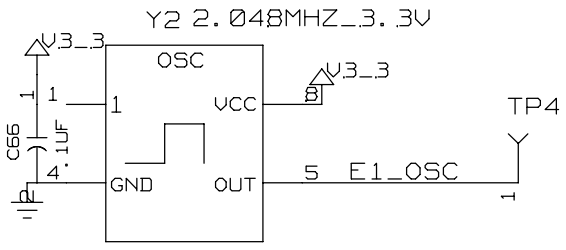
DESIGN KIT

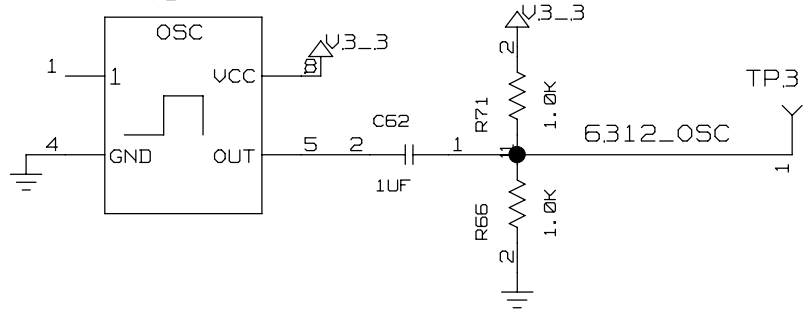
CONVERTED TO PDF: Fri Oct 20 10:08:32 2006

TITLE: DS26502DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 1 /14



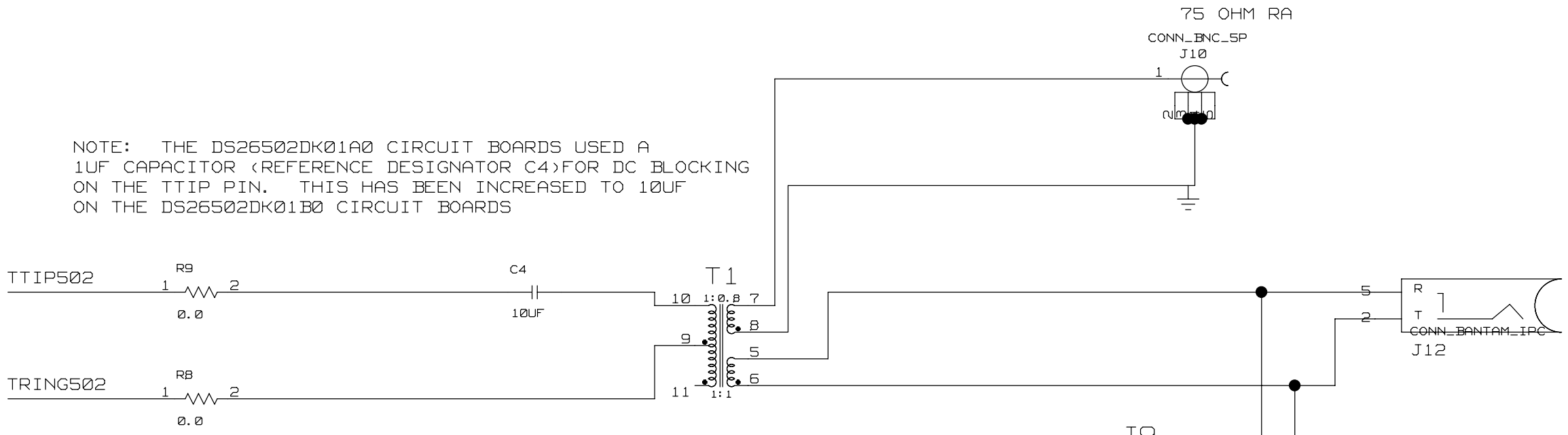




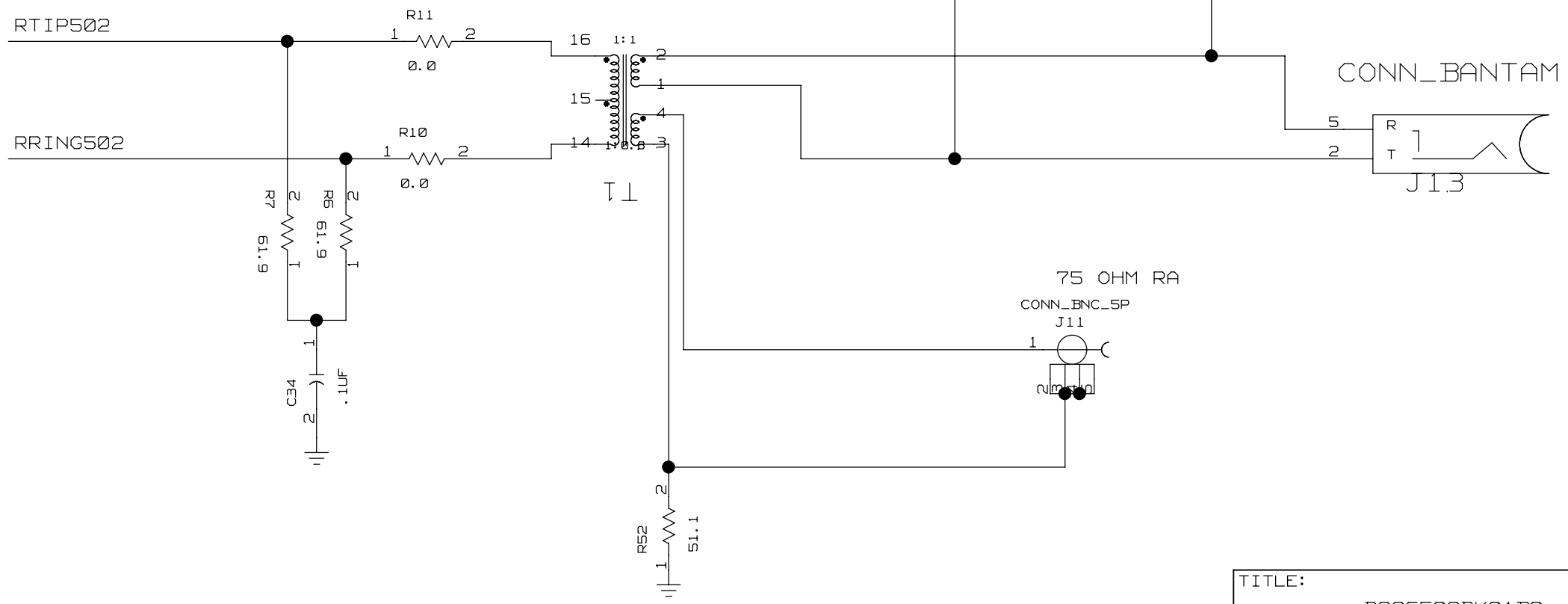


TITLE: DS26502DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 2 /14

NOTE: THE DS26502DK01A0 CIRCUIT BOARDS USED A 1UF CAPACITOR (REFERENCE DESIGNATOR C4)FOR DC BLOCKING ON THE TTIP PIN. THIS HAS BEEN INCREASED TO 10UF ON THE DS26502DK01B0 CIRCUIT BOARDS



NOTE: BOARD REVISIONS DS26502DK01A0 AND DS26502DK01B0 DO NOT USE THE CORRECT PIN NUMBERS ON THE RJ48 CONNECTOR (REFERENCE DESIGNATOR J9). THE RJ48 CONNECTOR SHOULD BE REMOVED SINCE IT HAS NON-STANDARD CONNECTION. THE SCHEMATIC HAS BEEN UPDATED AND IS CORRECT.



TITLE: DS26502DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 3 /14

TITLE: DS2650202DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 4 /14

INPUT CLOCKS

U4 XC2550_QFP I/O PORT

BANK 4

PD<31..16>

BANK 5

BANK 6

BANK 7

PA<15:0>

DAT502<7..0>

GCK3

BANK 0

BANK 1

BANK 2

ADDR502<7..0>

502 BUS MODE DETECTION

OUTPUT CLOCKS

MCLK502

TCLK502

TS_8K_4502

THZE502

RD#502

CS#502

WR#502

BIS0502

BIS1502

BTS502

X_INITXI

CFG_DINXI

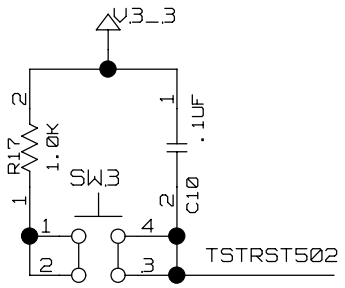
DS5 GREEN

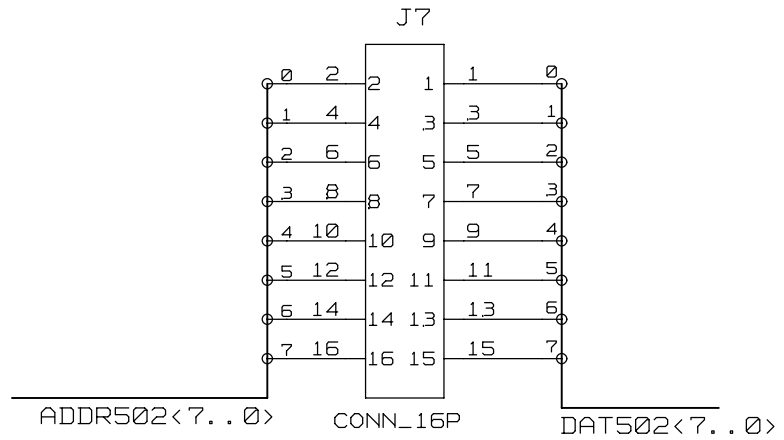
TIM_INTERUPT

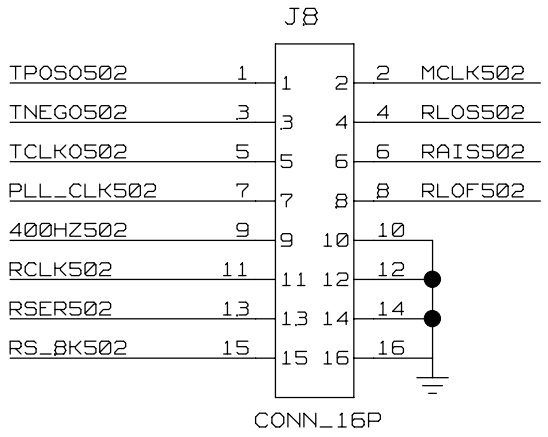
75 OHM VERT

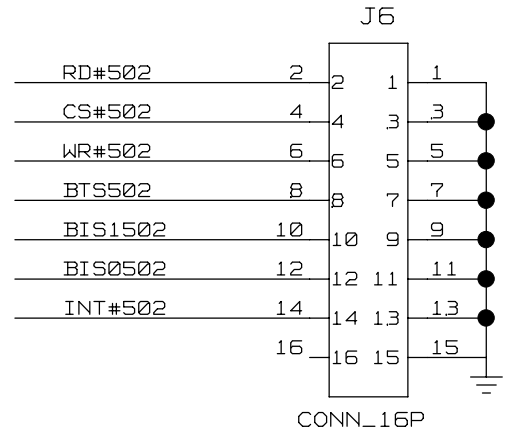
EXT_OSC

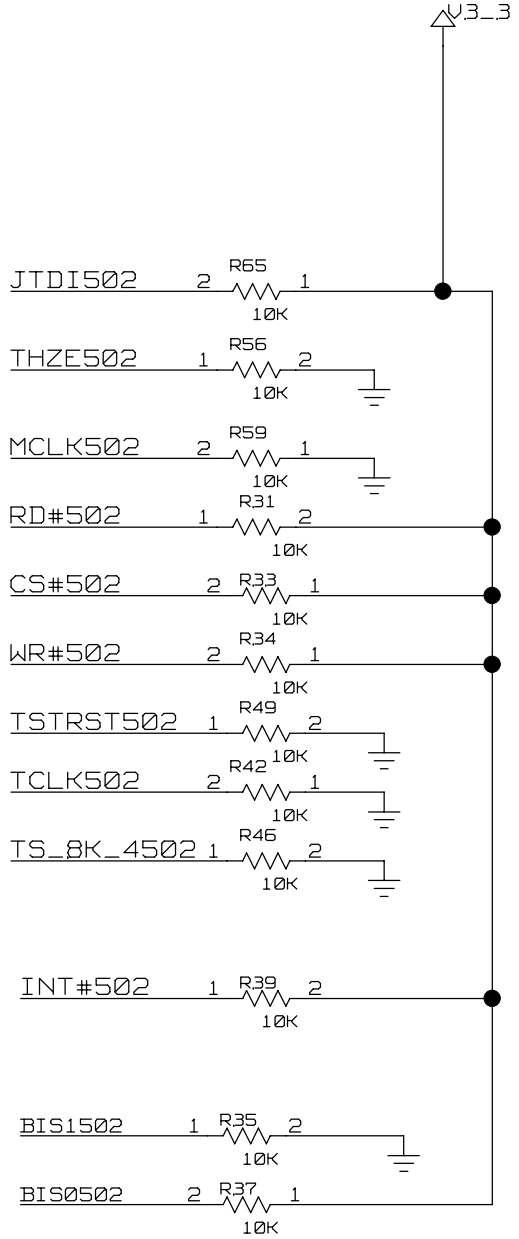
SPARE FPGA IO

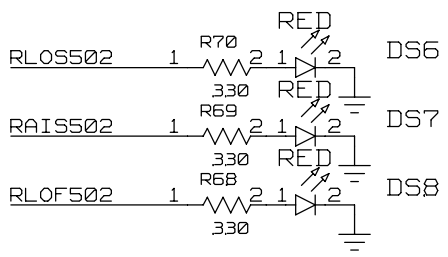






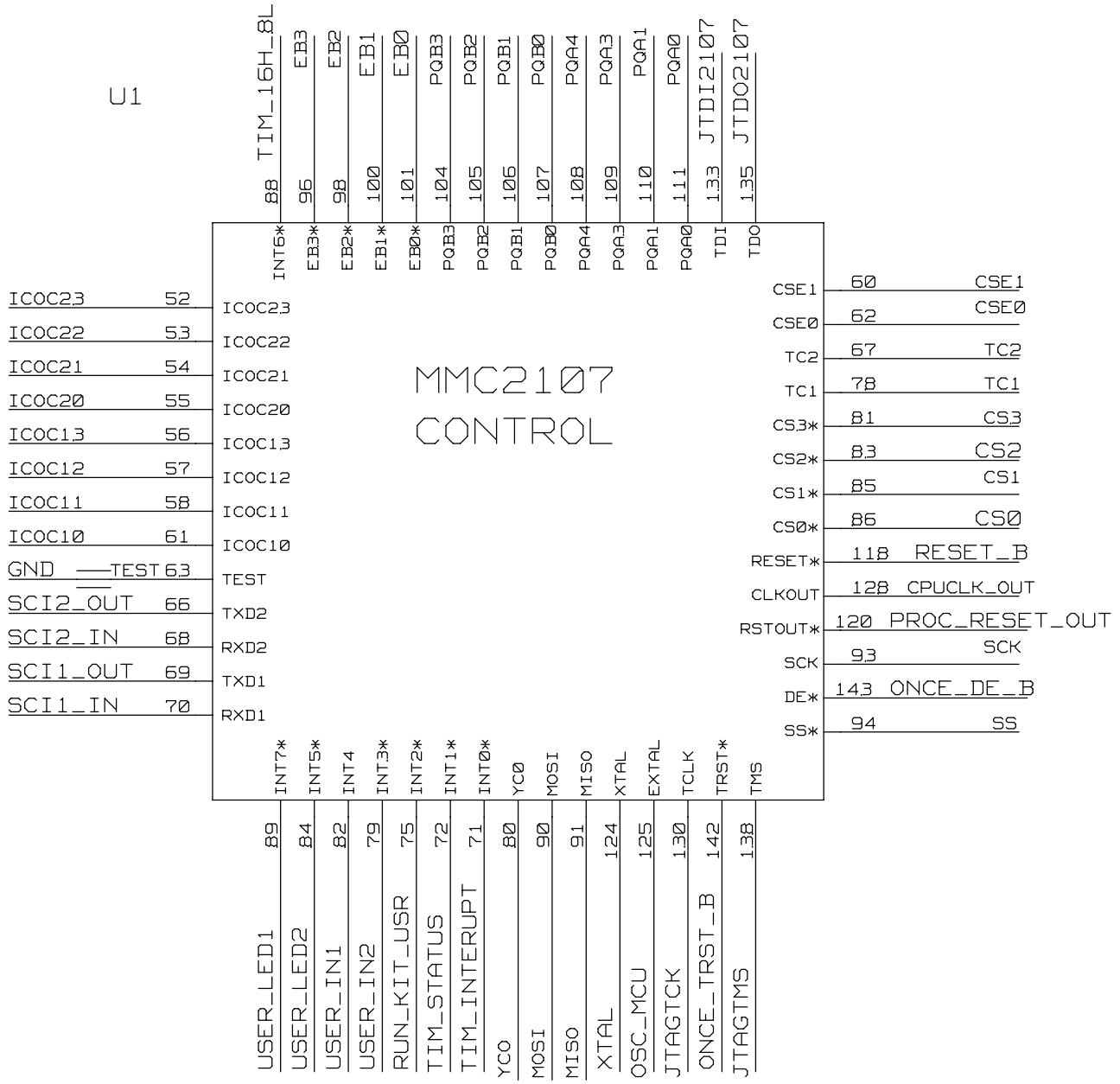


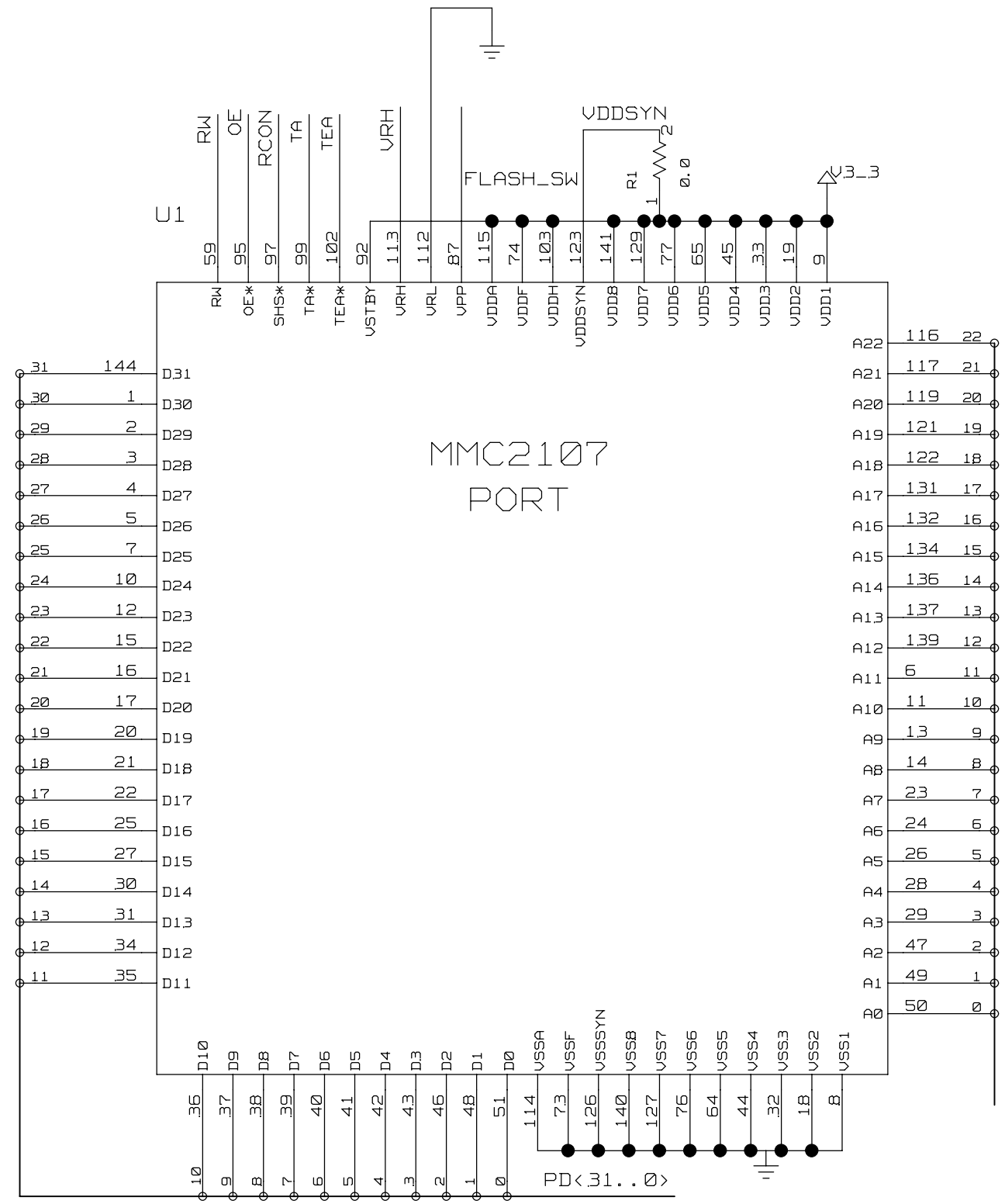




BIS[1:0] : 01 = PARALLEL PORT MODE
DEFAULT MODE (NON-MULTIPLEXED)

TITLE: DS26502DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 5 /14





TITLE: DS26502DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 6 /14

RESET CONFIGURATION

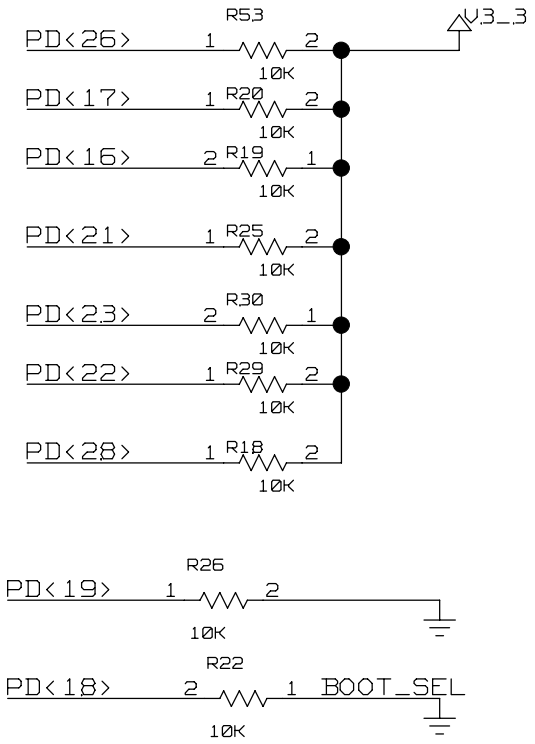
MASTER MODE

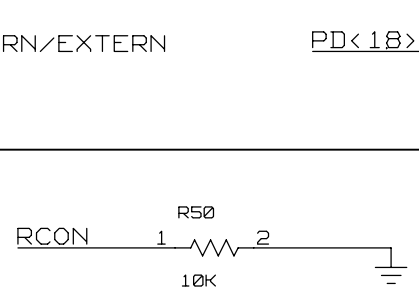
FULL DRIVE

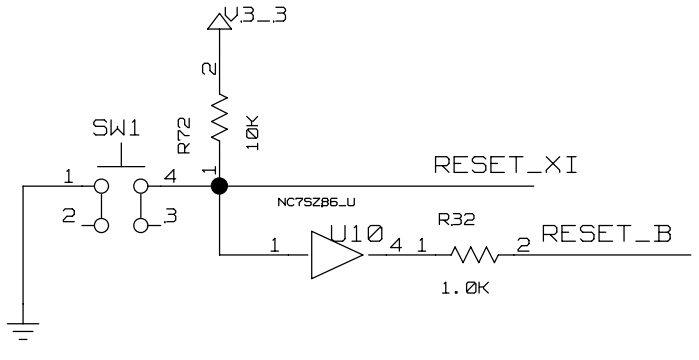
XTAL W/ PLL

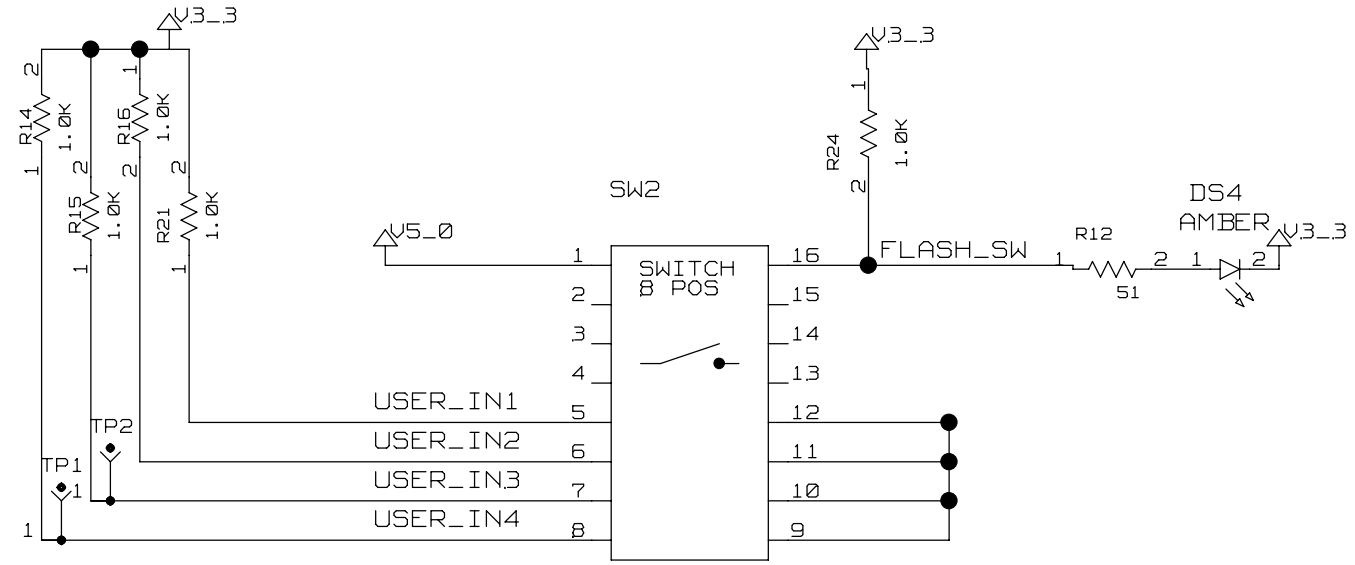
INTERNAL
FLASH ENABLE

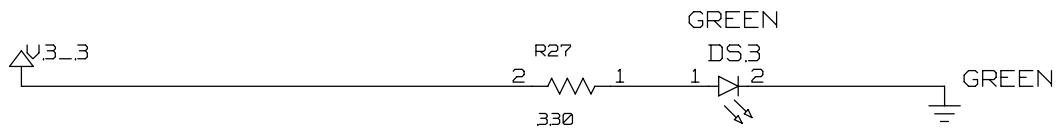
BOOT
INTERN/EXTERN

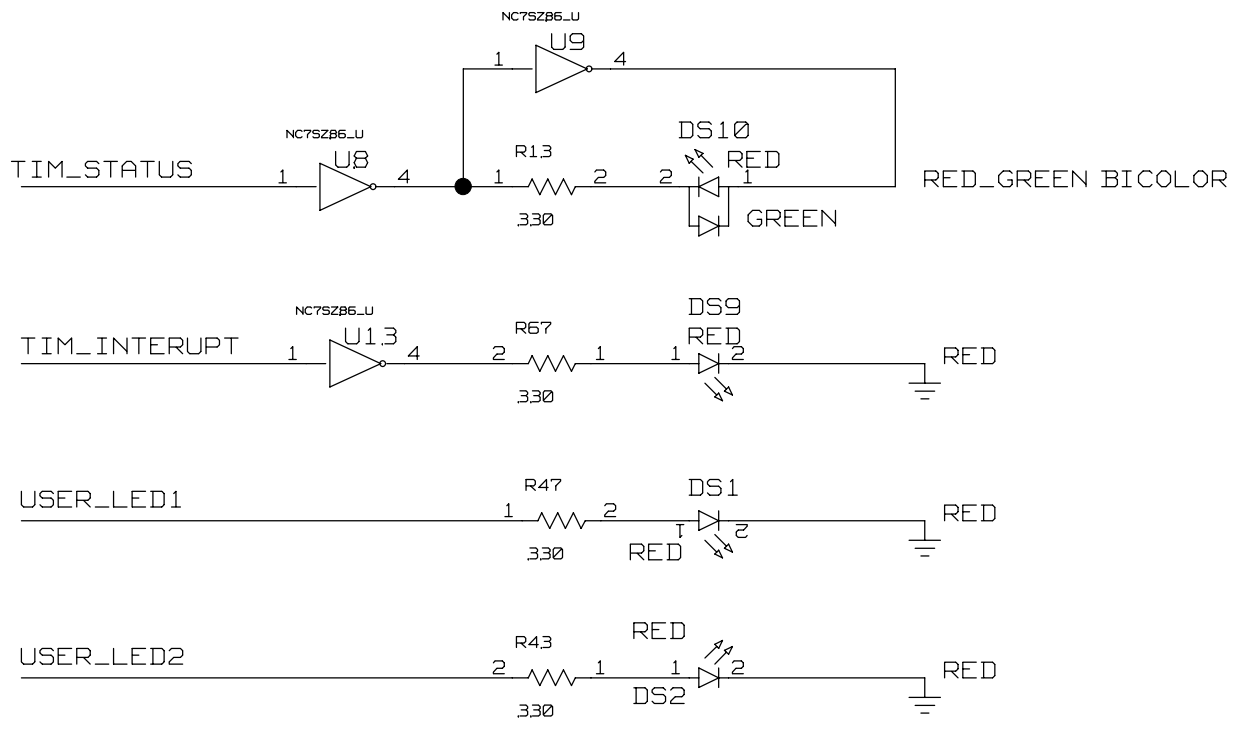






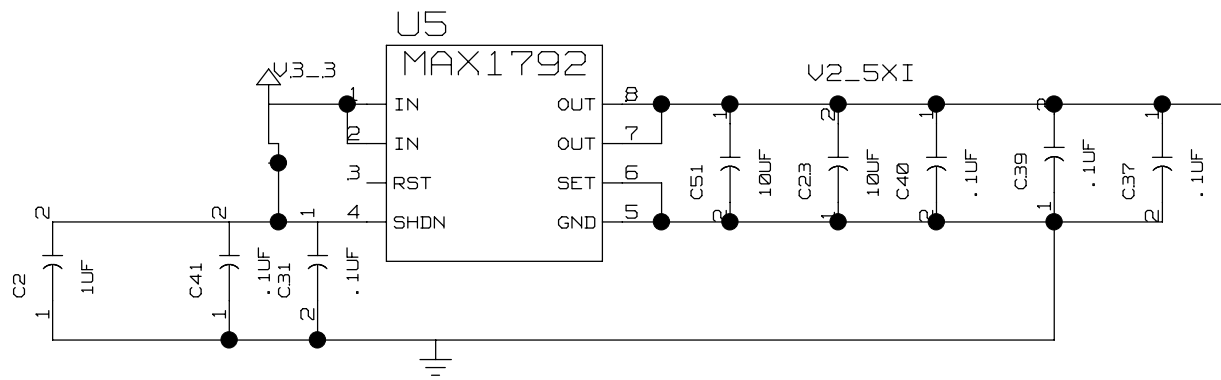


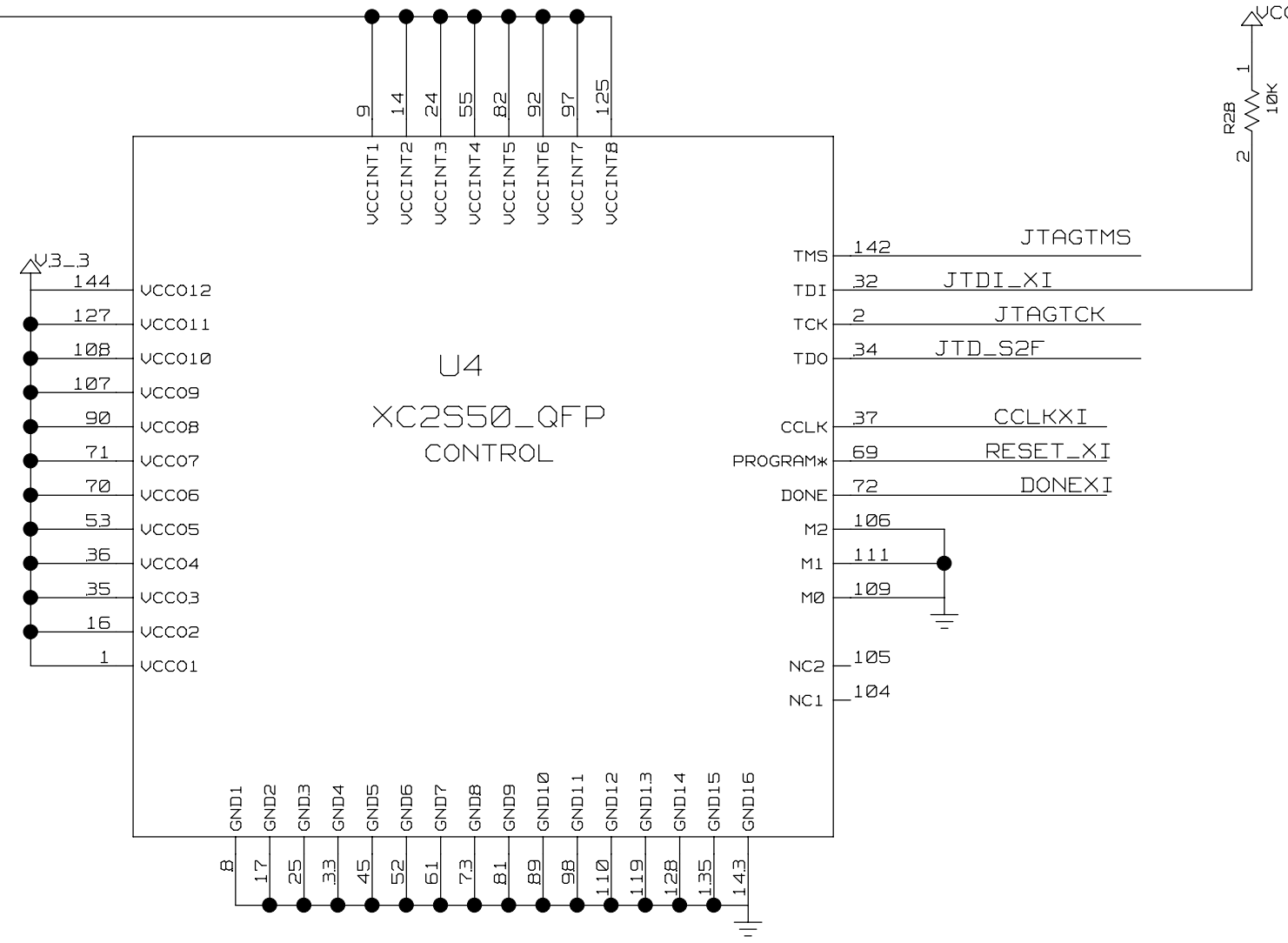


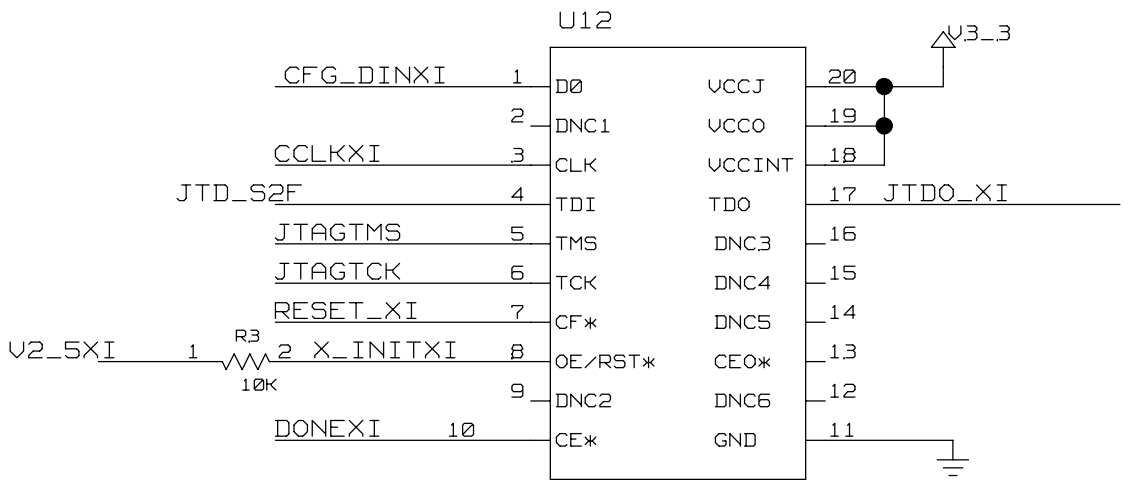


RESET AND CHIP CONFIGURATION

TITLE: DS26502DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 7 /14

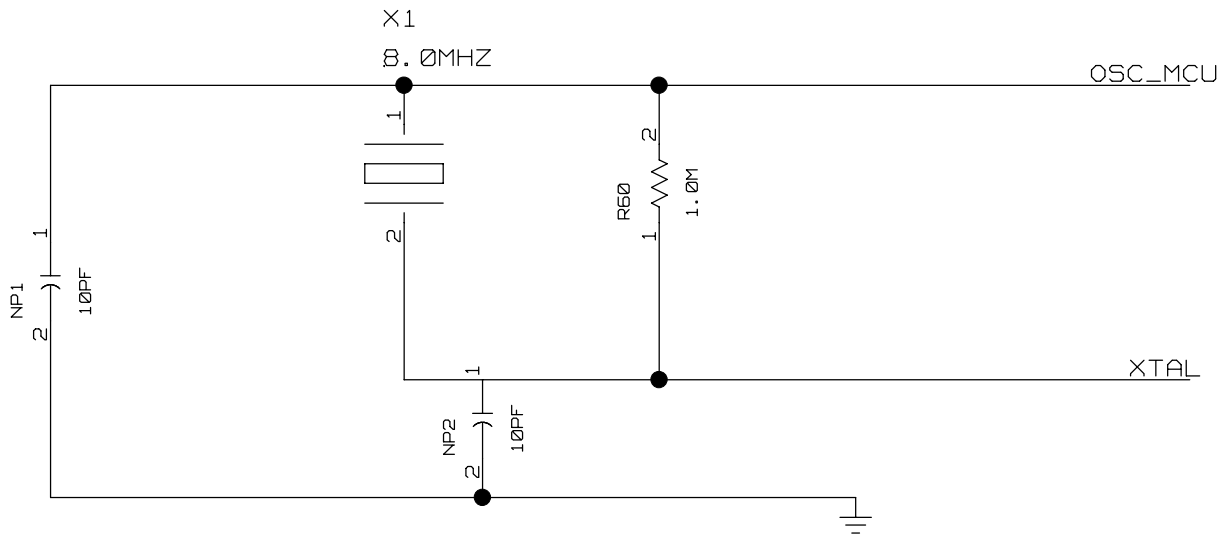




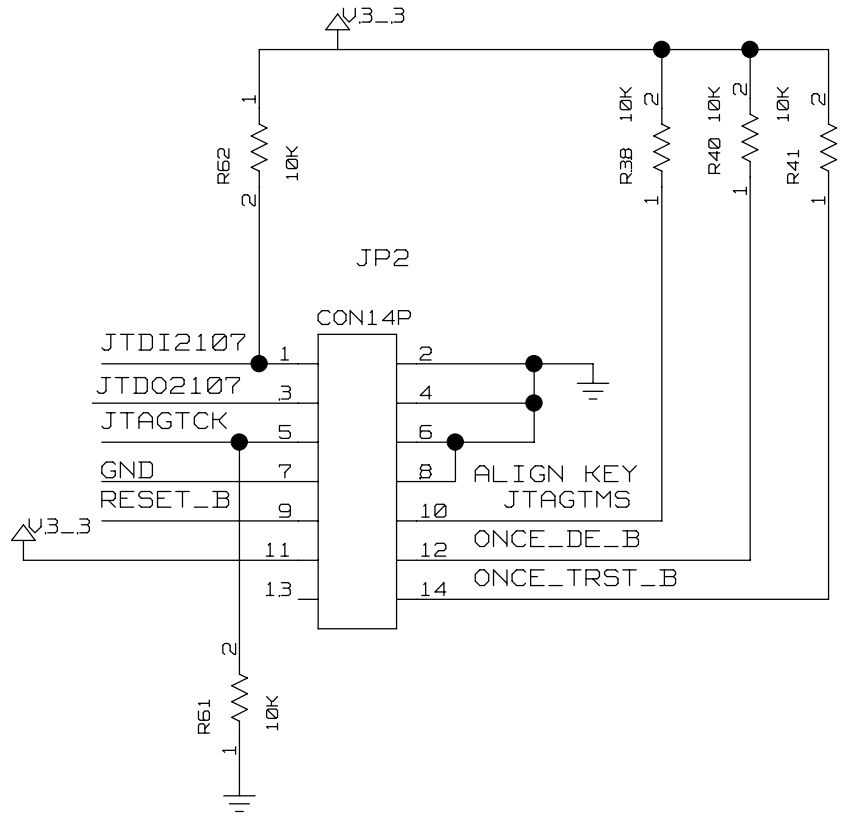


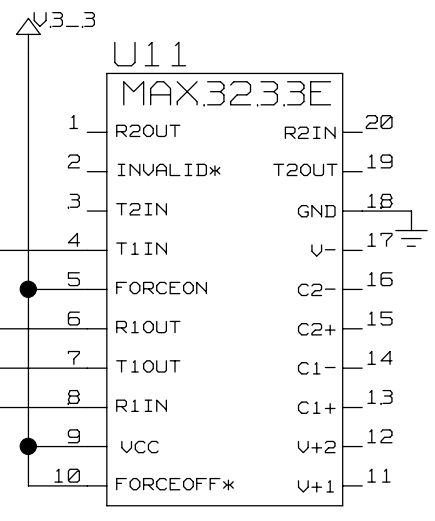
CLOCKS

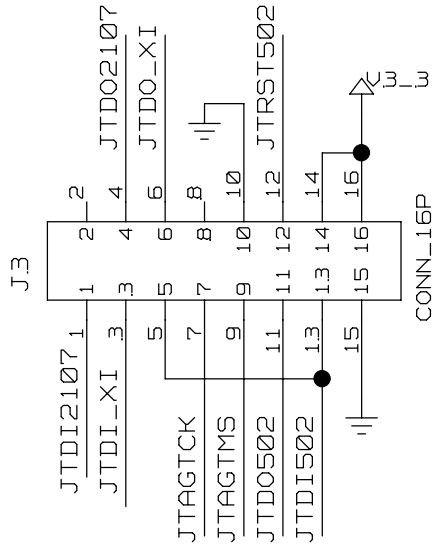
TITLE: DS26502DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 8 /14

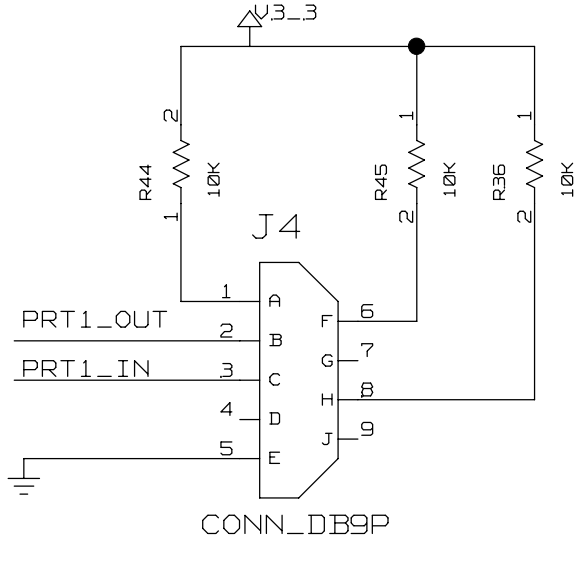


JTAG / ONCE
DEBUG SELECTION

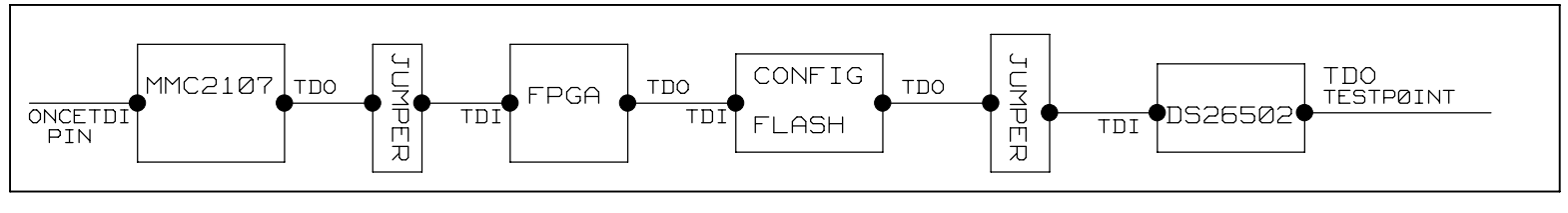




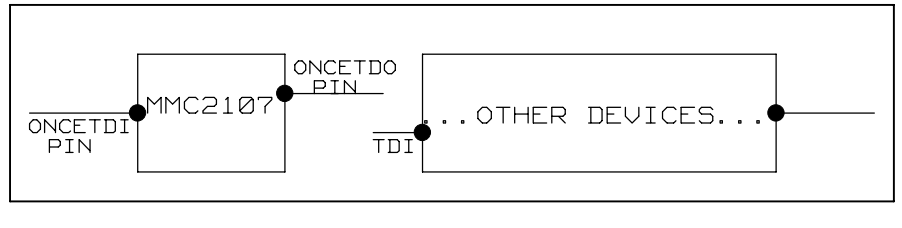




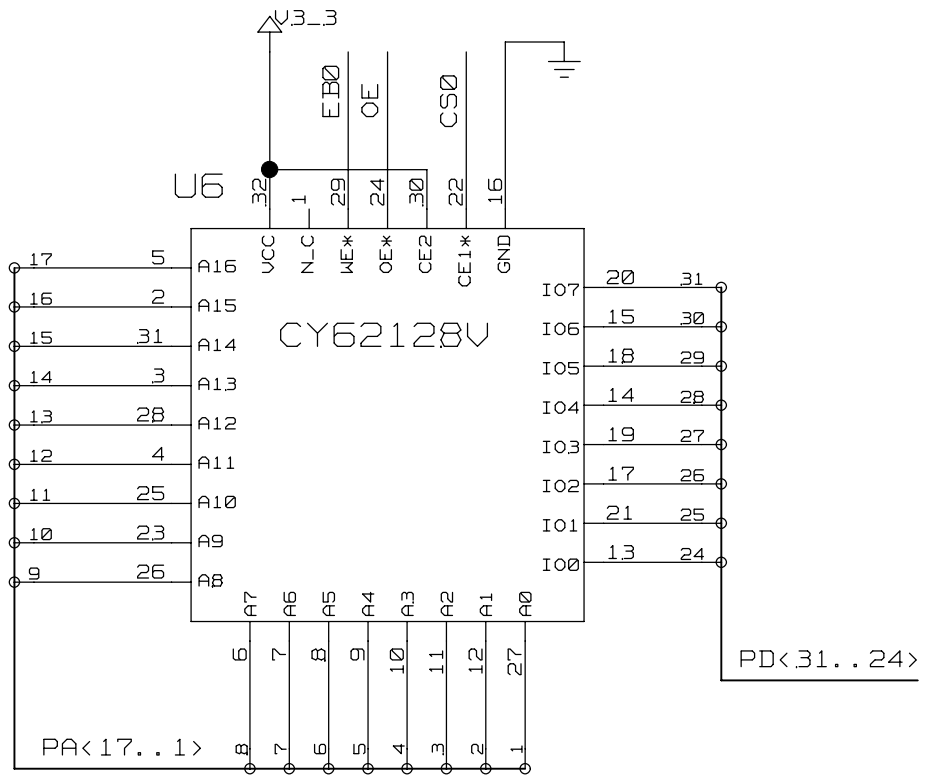
JTAG CONFIGURATION (BOUNDARY SCAN)

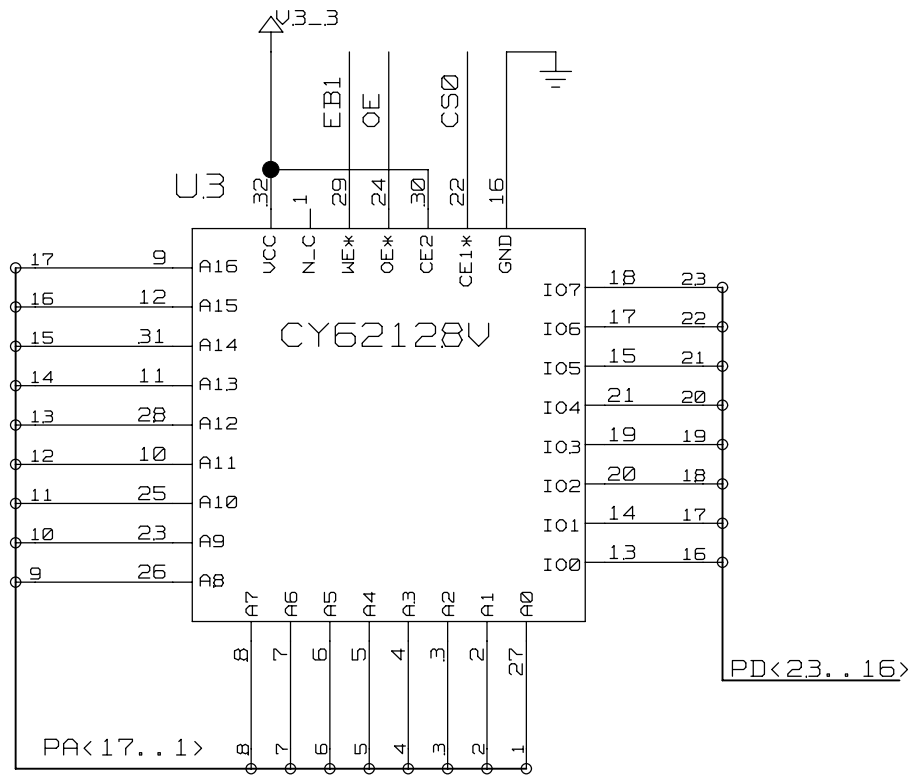


PROCESSOR DEBUG CONFIGURATION (ONCE)

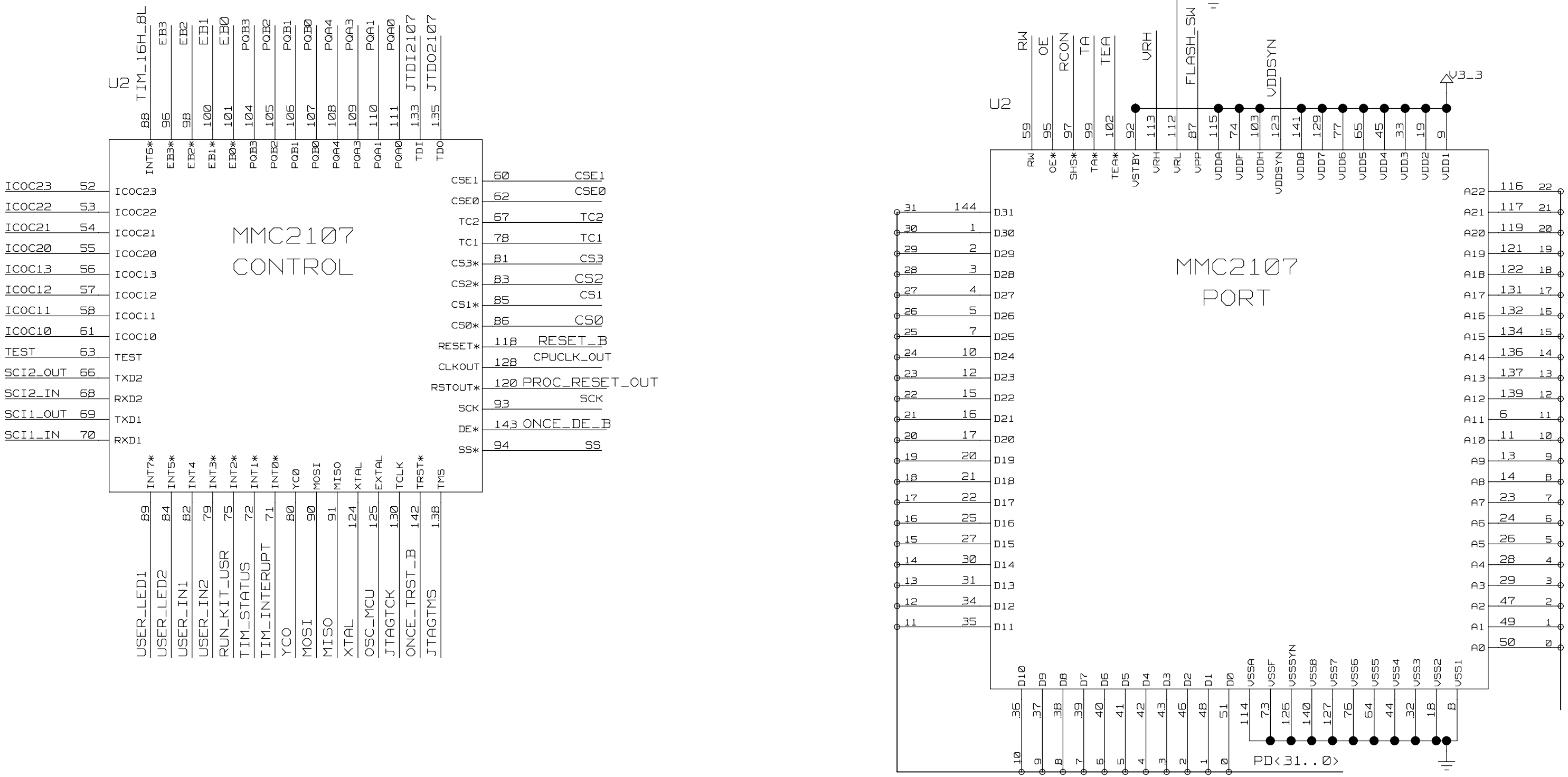


TITLE: DS26502DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 9 /14



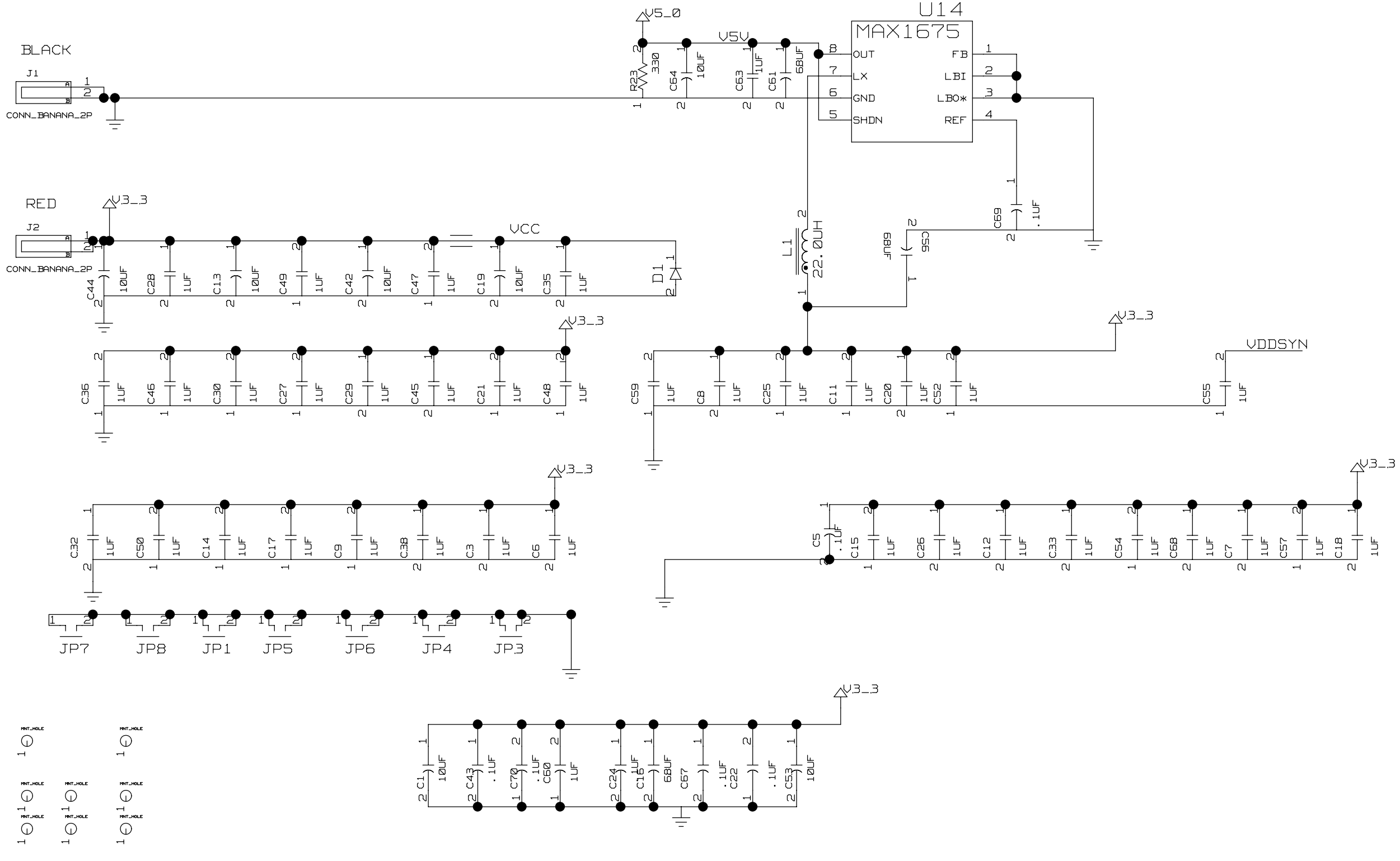


TITLE: DS26502DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 10/14



TEST-POINTS FOR PROCESSOR

TITLE: DS26502DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 11/14



TITLE: DS26502DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 12/14

*** Signal Cross-Reference for the entire design ***

400HZ502	4D6<> 5C8<> 2C8<
6312_OSC	2A1<> 4D6<>
ADDR502<7..0>	2C4> 4C1 5D4<
BIS0502	4A3<> 5B4<> 2C8< 5A2<
BIS1502	4A2<> 5B4<> 2C8< 5A2<
BOOT_SEL	7B6<
BTS502	4A2<> 5B4<> 2C8<
CCLKXI	8B7<> 8C1<
CFG_DINXI	4B2<> 8B7<>
CPUCLK_OUT	6B5<> 11B5<> 4C8<
CS#502	4A3<> 5B4<> 2C8< 5C2<
CS0	6B5<> 10D3<> 10D6<> 11C5<>
CS1	6C5<> 11C5<>
CS2	4A6<> 6C5<> 11C5<>
CS3	6C5<> 11C5<>
CSE0	6C5<> 11C5<>
CSE1	6C5<> 11C5<>
DAT502<7..0>	2C4> 5C2> 4C4
DONEXI	8A7<> 8B1<
E1_OSC	2B2<> 4D6<>
EB0	4B5<> 6D7<> 10D7<> 11D7<>
EB1	4B5<> 6D7<> 10D3<> 11D7<>
EB2	6D7<> 11D7<>
EB3	6D7<> 11D7<>
EXT_OSC	4D2<>
FLASH_SW	7D2<> 6D2< 11D3<
ICOC10	6B8<> 11B8<>
ICOC11	6B8<> 11C8<>
ICOC12	6C8<> 11C8<>
ICOC13	6C8<> 11C8<>
ICOC20	6C8<> 11C8<>
ICOC21	6C8<> 11C8<>
ICOC22	6C8<> 11C8<>
ICOC23	6C8<> 11C8<>
INT#502	2C8> 4B2<> 5B4<> 5B2<
JTAGTCK	6A6<> 8A7<> 9B4<> 9C3<> 11A6<> 2B8< 8C1<
JTAGTMS	6A6<> 8B7<> 9B4<> 9C2<> 11A6<> 2C8< 8C1<
JTDI502	9B4<> 2B8< 5C2<
JTDI2107	6D6<> 9B5<> 9C3<> 11D6<>
JTDI_XI	9B5<> 8C2<
JTDO502	2B8> 9B4<>
JTDO2107	6D6<> 9C3<> 9C5<> 11D6<>
JTDO_XI	8B5<> 9C5<>
JTD_S2F	8B7<> 8C1>
JTRST502	9C4<> 2B8<
MCLK502	5C7<> 2C8< 4A3< 5C2<
MCLK502XI	4A3<>
MISO	4A6<> 6A6<> 11A7<>
MOSI	4A6<> 6A6<> 11A7<>
OE	4A6<> 6D3<> 10D3<> 10D7<> 11D3<>
ONCE_DE_B	6B5<> 9B2<> 11B5<>
ONCE_TRST_B	6A6<> 9B2<> 11A6<>
OSC_MCU	6A6<> 9D5<> 11A6<>
PA<15..0>	4C4
PA<22..0>	6B1> 11A1>
PA<17..1>	10B4 10B7
PD<31..0>	6A2> 11A2>
PD<23..16>	10B2>
PD<31..16>	4B8 4B8
PD<31..24>	10B5>
PLL_CLK502	4D6<> 5C8<> 2C4<
PQA0	6D6<> 11D6<>
PQA1	6D6<> 11D6<>
PQA3	6D6<> 11D7<>
PQA4	6D6<> 11D7<>
PQB0	6D6<> 11D7<>
PQB1	6D7<> 11D7<>
PQB2	6D7<> 11D7<>
PQB3	6D7<> 11D7<>
PROC_RESET_OUT	4D6<> 6B5<> 11B5<>
PRT1_IN	9A8<> 9B8<
PRT1_OUT	9A8<> 9B8>
RAIS502	2B4> 5C7<> 5B8<
RCLK502	5B8<> 2C4<
RCON	6D3<> 11D3<> 7B8<
RD#502	4A3<> 5B4<> 2D8< 5C2<
RESET_B	6B5<> 9C3<> 11B5<> 7A6<
RESET_XI	7A7<> 8A7<> 8C1<
RLOF502	2B4> 5C7<> 5B8<
RLOS502	2B4> 5C7<> 5B8<
RRING502	2D8< 3B7<
RSER502	4B1<> 5B8<> 2C4<
RS_8K502	4D6<> 5B8<> 2C8<
RTIP502	2D8< 3B7<
RUN_KIT_USR	6A7<> 11A7<>
RW	4A6<> 6D3<> 11D3<>
SCI1_IN	6B8<> 9B8> 11B8<>
SCI1_OUT	6B8<> 11B8<> 9B8<
SCI2_IN	6B8<> 11B8<>
SCI2_OUT	6B8<> 11B8<>
SCK	4A6<> 6B5<> 11B5<>
SS	4A5<> 6B5<> 11B5<>
T1_OSC	2D2<> 4D6<>
TA	4A6<> 6D3<> 11D3<>
TC1	6C5<> 11C5<>
TC2	6C5<> 11C5<>
TCLK502	2C8< 4A3< 5B2<
TCLK502XI	4A3<>
TCLKO502	5C8<> 2C4<
TCSSI502	2C8<> 4D3<>
TEA	6D3<> 11D3<>
TEST	6B8<> 11B8<>
THZE502	4A3<> 2C8< 5C2<
TIM_16H_8L	6D7<> 11D8<>
TIM_INTERUPT	4B1> 6A7<> 7A4<> 11A7<>
TIM_STATUS	6A7<> 7B4<> 11A7<>
TMODE1502	4D3<> 2C8<
TMODE2502	4D3<> 2C8<
TNEGO502	2C4> 5C8<>
TPOSO502	2B4> 5C8<>
TRING502	2D4> 3C8<
TSER502	4B1<> 2C8<
TSTRST502	5D8<> 2C8< 5B2<
TS_8K_4502	4A3<> 2C8< 5B2<
TTIP502	2D4> 3C8<
USER_IN1	6A7<> 7C3<> 11A7<>
USER_IN2	6A7<> 7C3<> 11A7<>
USER_IN3	7C3<>
USER_IN4	7C3<>
USER_LED1	6A7<> 11A8<> 7A4<
USER_LED2	6A7<> 11A7<> 7A4<
V2_5XI	8D6<> 8A8<
V5V	12D4<>
VDDSYN	6D2< 11D2< 12C1<
VRH	6D3< 11D3<
WR#502	4A3<> 5B4<> 2C8< 5B2<
XTAL	6A6<> 9C5<> 11A7<>
X_INITXI	4A2<> 8A7<>
YCO	6A7<> 11A7<>

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*** Part Cross-Reference for the entire design ***

C1	CAP1	12A5
C2	CAP1	8C8
C3	CAP	12B5
C4	CAP	3D6
C5	CAP1	12B3
C6	CAP	12B5
C7	CAP	12B1
C8	CAP	12B4
C9	CAP	12B5
C10	CAP1	5D8
C11	CAP	12B3
C12	CAP	12B2
C13	CAP	12C6
C14	CAP	12B6
C15	CAP	12B3
C16	CAP1	12A4
C17	CAP	12B6
C18	CAP	12B1
C19	CAP	12C5
C20	CAP	12B3
C21	CAP	12B5
C22	CAP1	12A4
C23	CAP1	8C6
C24	CAP1	12A4
C25	CAP	12B3
C26	CAP	12B3
C27	CAP	12B6
C28	CAP	12C6
C29	CAP	12B5
C30	CAP	12B6
C31	CAP1	8C8
C32	CAP	12B7
C33	CAP	12B2
C34	CAP1	3A6
C35	CAP	12C4
C36	CAP	12B7
C37	CAP1	8C5
C38	CAP	12B5
C39	CAP1	8C6
C40	CAP1	8C6
C41	CAP1	8C8
C42	CAP	12C5
C43	CAP1	12A5
C44	CAP	12C7
C45	CAP	12B5
C46	CAP	12B6
C47	CAP	12C5
C48	CAP	12B4
C49	CAP	12C6
C50	CAP	12B6
C51	CAP1	8C7
C52	CAP	12B3
C53	CAP1	12A3
C54	CAP	12B2
C55	CAP	12B1
C56	CAP	12C3
C57	CAP	12B1
C58	CAP1	4D1
C59	CAP	12B4
C60	CAP1	12A4
C61	CAP	12D3
C62	CAP1	2A2
C63	CAP	12D4
C64	CAP	12D4
C65	CAP1	2D3
C66	CAP1	2B3
C67	CAP1	12A4
C68	CAP	12B2
C69	CAP1	12C2
C70	CAP1	12A5
D1	DIODE	12C4
DS1	LED	7A3
DS2	LED	7A3
DS3	LED	7B3
DS4	LED	7D1
DS5	LED	4B1
DS6	LED	5B7
DS7	LED	5B7
DS8	LED	5B7
DS9	LED	7B3
DS10	LED2	7B3
J1	CONN_BANANA_2P	12D7
J2	CONN_BANANA_2P	12C7
J3	CONN_16P	9B5
J4	CONN_DB9P	9A7
J5	CONN_BNC_5P	4D1
J6	CONN_16P	5B3
J7	CONN_16P	5D3
J8	CONN_16P	5C7
J9	CONN_RJ48	3B4
J10	CONN_BNC_5P	3D3
J11	CONN_BNC_5P	3A4
J12	CONN_BANTAM_IPC	3C2
J13	CONN_BANTAM	3B2
JP1	JMP	12B6
JP2	CON14P	9C2
JP3	JMP	12B5
JP4	JMP	12B5
JP5	JMP	12B6
JP6	JMP	12B5
JP7	JMP	12A7
JP8	JMP	12A6
L1	COIL_2P	12C3
MNT_HOLE1	MNT_HOLE	12A6
MNT_HOLE2	MNT_HOLE	12A6
MNT_HOLE3	MNT_HOLE	12A7
MNT_HOLE4	MNT_HOLE	12A6
MNT_HOLE5	MNT_HOLE	12A7
MNT_HOLE6	MNT_HOLE	12A7
MNT_HOLE7	MNT_HOLE	12A7
MNT_HOLE8	MNT_HOLE	12A7
NP1	CAP	9C8
NP2	CAP	9C7
R1	RES1	6D2
R2	RES1	4B1
R3	RES1	8A7
R4	RES1	4A3
R5	RES1	4A3
R6	RES1	3B6
R7	RES1	3B6
R8	RES1	3C7
R9	RES1	3D7
R10	RES1	3B6
R11	RES1	3B6
R12	RES1	7D1
R13	RES1	7B3
R14	RES1	7D4
R15	RES1	7D4
R16	RES1	7D4
R17	RES1	5D8
R18	RES1	7C7
R19	RES1	7D7
R20	RES1	7D7
R21	RES1	7D4
R22	RES1	7C7
R23	RES1	12D4
R24	RES1	7D2
R25	RES1	7D7
R26	RES1	7C7
R27	RES1	7C3
R28	RES1	8C1
R29	RES1	7C7
R30	RES1	7C7
R31	RES1	5C1
R32	RES1	7A7
R33	RES1	5C1
R34	RES1	5C1
R35	RES1	5A1
R36	RES1	9A7
R37	RES1	5A1
R38	RES1	9C1
R39	RES1	5B1
R40	RES1	9C1
R41	RES1	9C1
R42	RES1	5B1
R43	RES1	7A3
R44	RES1	9A7
R45	RES1	9A7
R46	RES1	5B1
R47	RES1	7A3
R48	RES1	2C7
R49	RES1	5B1
R50	RES1	7B8
R51	RES1	2C4
R52	RES	3A5
R53	RES1	7D7
R54	RES1	2C4
R55	RES1	2C8
R56	RES1	5C1
R57	RES1	2C5
R58	RES1	2C4
R59	RES1	5C1
R60	RES1	9D6
R61	RES1	9B2
R62	RES1	9C2
R63	RES1	4D2
R64	RES1	4D2
R65	RES1	5C1
R66	RES1	2A2
R67	RES1	7A3
R68	RES1	5B7
R69	RES1	5B7
R70	RES1	5B7
R71	RES1	2A2
R72	RES1	7A8
SW1	PUSHBUTTON	7A8
SW2	SWITCH_8POS	7D2
SW3	PUSHBUTTON	5D8
T1	XFMR_2IN_4OUT_U	3B5 3D5
TP1	TESTPOINT_1P	7C4
TP2	TESTPOINT_1P	7C4
TP3	TESTPOINT	2A1
TP4	TESTPOINT	2C2
TP5	TESTPOINT	2D2
TP6	TESTPOINT	4D2
TP7	TESTPOINT	4D2
TP8	TESTPOINT	4D3
TP9	TESTPOINT	4D2
TP10	TESTPOINT	4D3
U1	MMC2107	6D3 6D8
U2	MMC2107	11C4 11D8
U3	CY6212BV	10C4
U4	XC2S50_QFP	4C3 4C6 8C3
U5	MAX1792	8D7
U6	CY6212BV	10C7
U7	DS26502_U1	2C6
U8	NC7SZ86_U	7B4
U9	NC7SZ86_U	7B3
U10	NC7SZ86_U	7A7
U11	MAX3233E	9B7
U12	XILINX_XCF01S	8B7
U13	NC7SZ86_U	7A4
U14	MAX1675	12D3
X1	XTAL	9D7
Y1	OSC1	2A3
Y2	OSC1	2C3
Y3	OSC1	2D3

REVISION HISTORY:

041205 - INITIAL RELEASE OF 01B0 VERSION.
THIS VERSION IS EXACTLY LIKE THE 01A0 VERSION EXCEPT FOR THE FOLLOWING:
- SIGNAL RCLK502 WAS CONNECTED TO THE FPGA, U4, AT PIN 63.
- THE PINS WERE SWAPPED ON C13, C42 & C61

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